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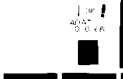

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FINAL TECHNICAL REPORT

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This report documents the feasibility of modifying and repackaging the Solid State Power Controller (SSPC) developed for the B-1 to meet the performance and configuration requirements for Advanced Aircraft Electrical Systems (AAES).

The effort included an analysis of the applicability of the B-1 monolithic and pass elements, and the application of advance developments to meet the volumetric constraints of NADC-30-TS-7602.

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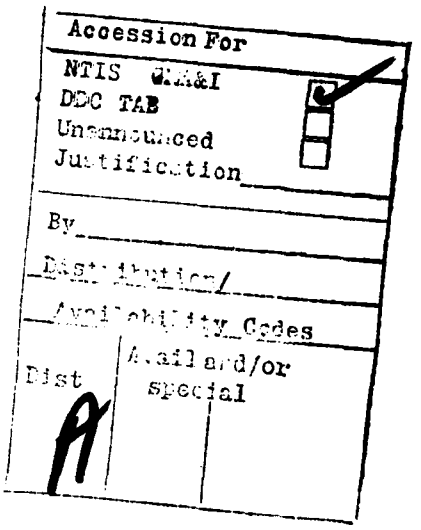
Preface

This document is the technical report for the B-1 Power Controller Feasibility Study. The effort was performed by Autonetics Strategic Systems Division of Rockwell International Corporation, Anaheim, California, under Naval Air Devleopment Center Contract Number N62269-79-C-0294.



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I. SUMMARY

This report documents the results of the B-1 Power Controller Feasibility Study performed by the Autonetics Strategic Systems Division (ASSD) of Rockwell International on Contract N62269-79-C-0294.

The objective of this study was to determine the feasibility of modifying Solid State Power Controllers (SSPC's) developed for the B-1 to meet the performance and configuration requirements of the Advanced Aircraft Electrical System (AAES).

The design described in this report uses the B-1 monolithic and pass elements. The physical and thermal constraints necessitated a repackage of the B-1 functions as well as remechanizations to eliminate the bulky magnetic components and capacitors.

Most of the functional requirements of the specification are satisfied with the proposed mechanization. Some of the requirements, e.g. turn on/off delays and trip curve slope, that are inherent in the monolithic require modification.

The B-1 monolithic fabrication process, metal gate, has been replaced with a silicon gate process. The new process provides a higher device yield along with the improved functional capability. A conversion of the monolithic to the new process is recommended for future applications.

II. INTRODUCTION

2.1 Background

The Rockwell SSPC, Appendix A, was designed as a modular assembly to mechanize B-1 230 Vac, 400 Hz, 2 amp power controller requirements. It was fully developed and ready for production verification testing at the time the B-1 Program was terminated. The technology applied to this program advanced the state-of-the-art in ac power controllers. The objective of this contract was to determine the applicability of this technology to AAES power controller requirements.

2.2 Study Requirements

The goal of this study was to apply the monolithic device, Appendix B, developed for the B-1 SSPC, to a design applicable to the AAES power controllers. Specification No. NADC-30-TS-7602 of 27 April 1976, with updates, provided the design criteria.

Specific requirements included:

- Developing a Solid State Electric Logic (SOSTEL) compatible interface
- Applicability of the B-1 SSPC pass elements
- Compliance with Specification NADC-30-TS-7602
- Development of a packaging concept
- A reliability prediction
- A study of the possibility of utilizing other B-1 SSPC hardware for AAES applications

2.3 Study Approach

The B-1 modular SSPC design was initially modified to satisfy AAES functional requirements, with minimum change to the B-1 packaging concept. The AAES packaging constraints were then applied. The component volumetric requirements exceeded the design constraints, so the B-1 SSPC was remechanized to reduce/eliminate the bulky components.

Once a remechanization was achieved, it was apportioned to physical assemblies that would meet the AAES constraints. A thermal analysis and reliability prediction was performed on the resultant configuration.

The results of this study are documented in this report.

III. TECHNICAL DISCUSSION

3.1 Modular Mechanizations

3.1.1 Objective. Modify the design of the ASSD B-1 SSPC, Part Number 12880-507-1, to be a 115 Vac quadruple SSPC unit, with a SOSTEL compatible interface.

3.1.2 115 Vac Primary Power Modifications. The ASSD SSPC Unit, Appendix A, contains four identical PC's operating from 230 Vac primary power. Referring to Figure 1, the modification for 115 Vac requires a change to the input power transformer (1), and a change in the voltage sense resistor divider network (2). Neither of the hybrids are impacted by these changes.

The "power transformer" in Figure 1 is used for internal SSPC power. The primary winding, the only common element of the 4 SSPC's, will have its primary turns reduced by 50% and a potential wire size increase. This change will maintain the internal power supplies at (+) and (-) 12 volts dc.

The second change required for 115 Vac operation is in the voltage sense resistors. The voltage sense network is used in determining "status" of the power controller, and is not involved in the control or trip functions.

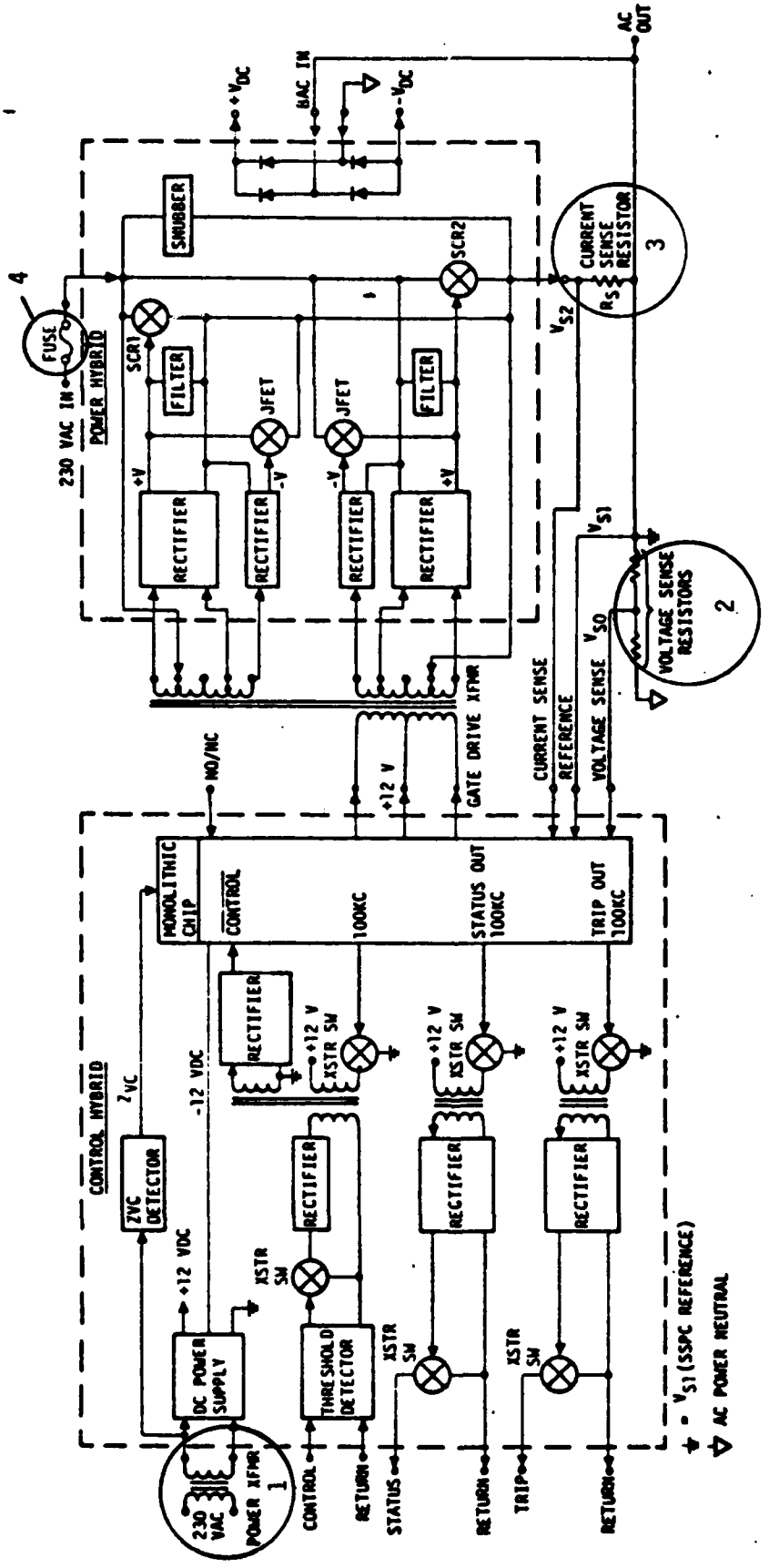


Figure 1. SSPC - Function Flow Diagram

For 230 Vac, it is set to sense voltage-to-the-load $\geq$ 160 V. For a 115 Vac SSPC, the sense will be set to approximately 80 V. Neither the resistor nor the transformer modification will impact the physical design of the module.

The preceding changes are all that are required to provide 2 amp 115 Vac capability.

3.1.3 Ampacity Changes. The 115 Vac modifications described in Paragraph 3.1.2 provide an SSPC with capability of up to 2 amps. Referring to Figure 1, there are two areas, the current sense resistor (3) and the fail safe fuse (4) that change for the 5 amp current rating. A current sense resistor value would be selected to rescale the power controller for the desired rating. The new resistor would be physically interchangeable with the existing one.

Fuse redesign is required for fail safe protection of aircraft wiring. The fuse characteristics are based on wire size and power control rating, Figure 2. The fuse presently used is a unique ASSD design, Figure 3, for the protection of #26 gauge wire and a power controller rated at 2 amps. The same design techniques are required if other wire sizes are used, or if the SSPC rating is greater than 3 amps. The new fuse would be physically interchangeable with the existing one.

Other areas of the modular power controller design that could be impacted by 5 amp requirements are the gate drive to the SCR's, the printed circuit line width, and the heat rail.

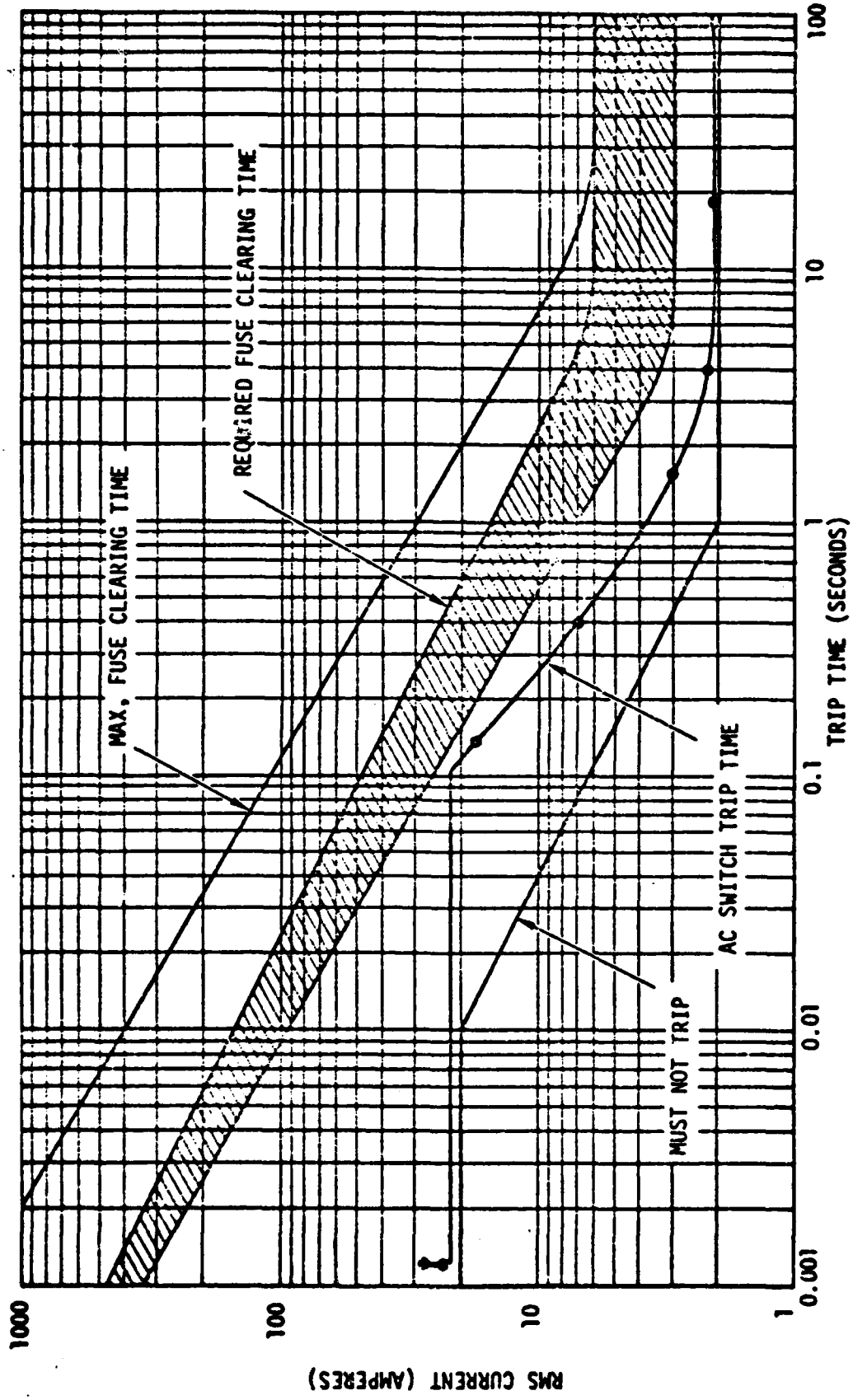


Figure 2. Fuse - Clearing Time

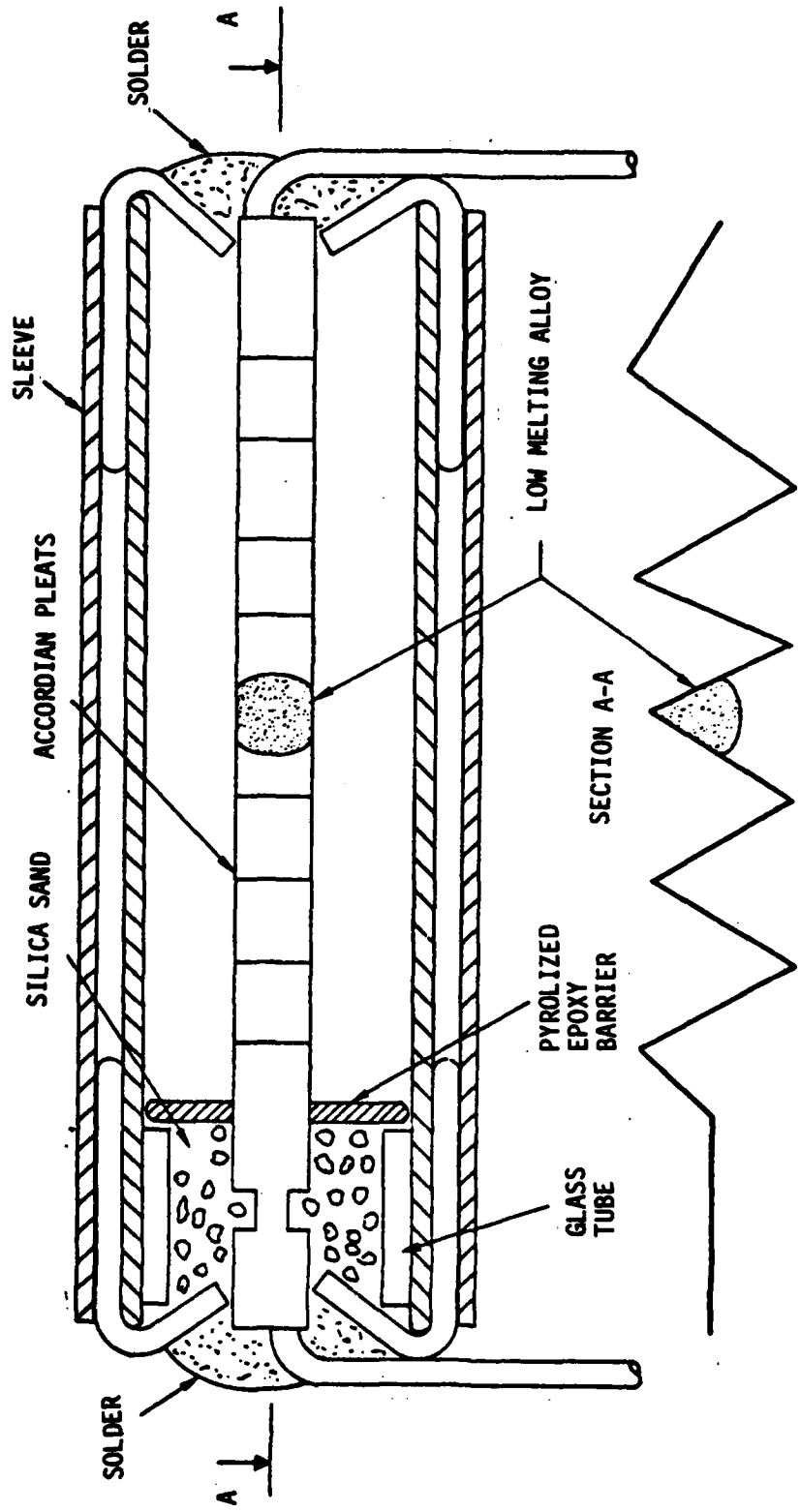


Figure 3. Fuse - Autonetics Design

3.1.4 SOSTEL Interface. The SOSTEL System employs a bi-directional, impedance change interface technique. The ASSD SSPC Unit has individual command, trip and status lines. One technique for transforming the interface to be SOSTEL compatible is shown in Figure 4. It requires the addition of three resistors per circuit or 12 per module. The interface modifications would be a part of the Control Hybrid, Figure 5. The SOSTEL type interrogation system would operate as follows.

3.1.4.1 Status Indication. The Status Indication (R = 720 ohms) would be provided by selecting R_S from the relationship $720 = \frac{1.1K\ (R_S)}{1.1K + R_S}$. Resistor R_C is derived from the relationship $1.1K = \frac{R_C\ R_{in}}{R_C + R_{in}}$, where R_{in} is equal to the input resistance of the control input; R_{in} is approximately equal to $R_{in} = \frac{5v}{3.3\ mA} = 1.5K$.

3.1.4.2 Trip Indication. The Trip Indication (R = 420 ohms) would be achieved by selecting R_T from the relationship $420 = \frac{1.1K\ (R_T)}{1.1K + R_T}$.

3.1.4.3 Fault Indication. The B-1 monolithic generates a status term that is indicative of voltage applied to the load and that the SCR's are not half-waving. This status term is independent of the input command signal. Thus, as a result, it is not possible to generate a fault impedance when the main elements are shorted and the controller interrogated by the 50 μsec pulse.

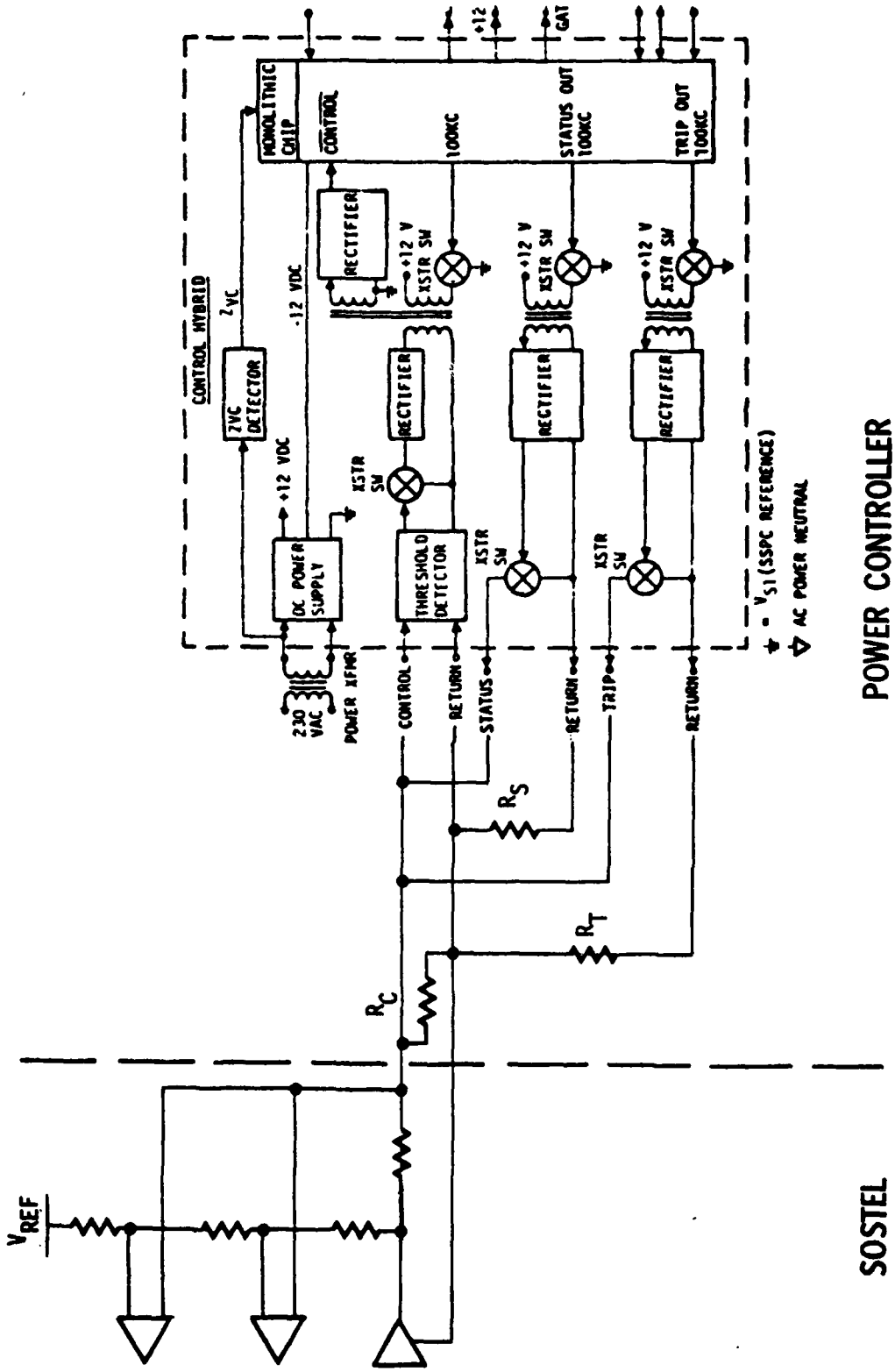


Figure 4. SOSTEL SSPC Interface

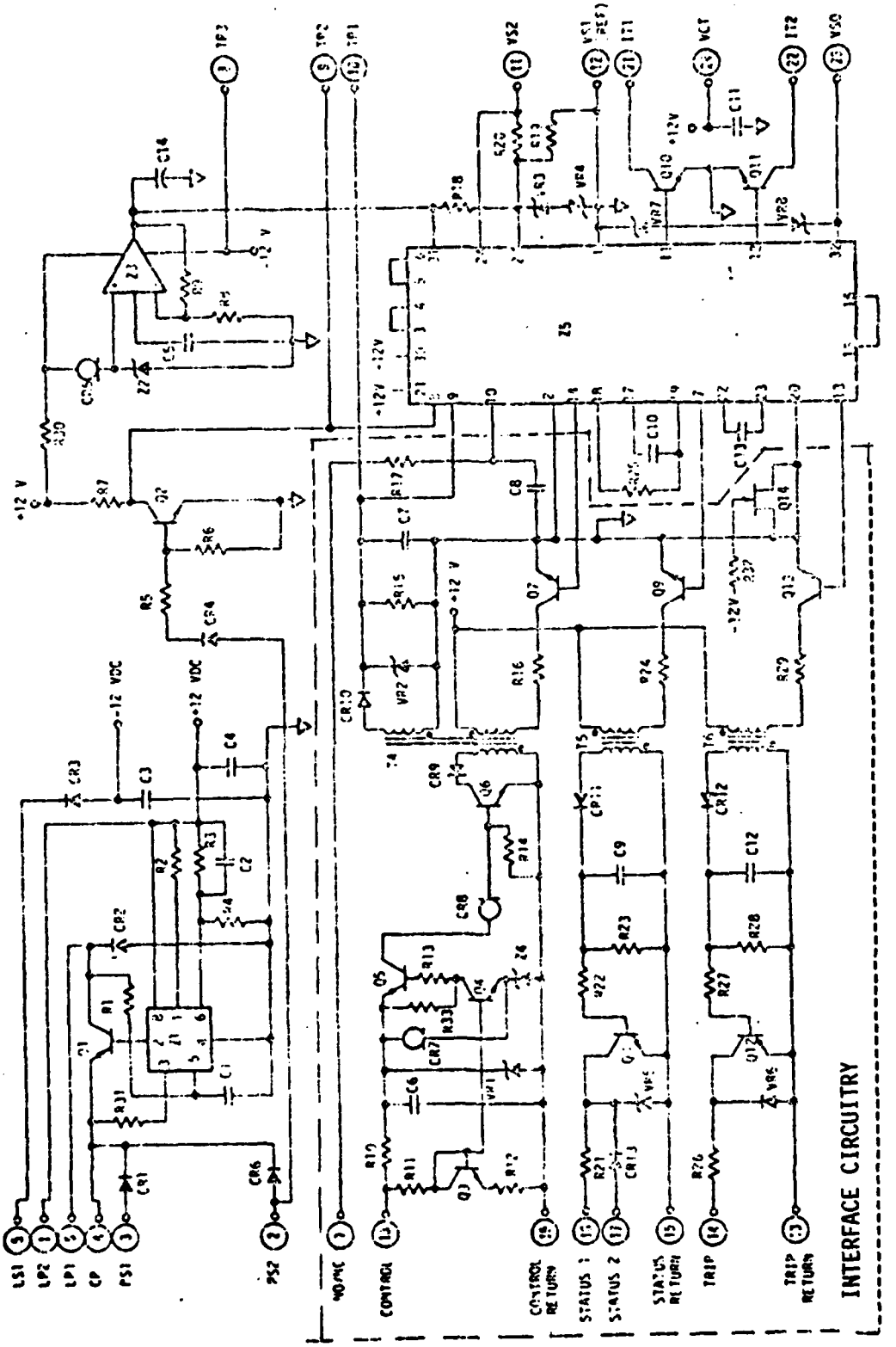


Figure 5. Control Hybrid Schematic

This mechanization also prevents indicating a normal impedance when turned off and interrogated by the 50 μsec pulse. A normal impedance would be indicated when the power controller is commanded on.

The present current monitoring mechanization does not indicate if current is less than 10% or less of rated. It is therefore not possible to indicate a fault impedance when current is 10% or less of rated.

A fault impedance would be indicated if no bus voltage is present for either command state.

Additional logic mechanizations are required along with improved current sensing in order to mechanize a complete SOSTEL interface.

3.1.4.4 Remechanization of B-1 SSPC. The preceding are the changes that would be required to the B-1 SSPC for AAES 115 V applications, retaining the maximum commonality, i.e. modular packaging concepts, with the existing B-1 design. The modular packaging concept was selected for the B-1 based on cost of ownership studies.

A remechanization feasibility study of the B-1 SSPC was performed to reduce or eliminate the magnetic components and capacitors. For the AAES requirements, within the envelope constraints of 1.5" X 1.5" X 1.1", the changes are discussed in the following section of this report.

3.2 AAES Mechanization

The B-1 circuit designs were examined and simplified in the following areas.

- SOSTEL interface circuits were developed
- SCR drive circuitry was simplied to make use of advances in microcircuit technology since the B-1 design time frame
- An improved power supply design reduced the physical size of large magnetic components and large capacitors

3.2.1 General Description. Figure 6 illustrates, in block diagram form, the control circuit, power switch circuits and their relationship within a complete SSPC. Figure 7 shows the control circuit in schematic form. The control circuit contains a B-1 monolithic integrated circuit and interface circuitry for SOSTEL.

3.2.2 Monolithic. The B-1 monolithic (Z5) contains the major timing and control functions for the SSPC. A functional description of the monolithic is presented in Appendix B.

It provides, on a single chip, full cycle control of power. In response to an external "turn on" control signal, the SSPC monolithic turns on at the zero voltage point where the ac input voltage is positive going, similarly, in response to a "turn off" control signal, the device turns off at the zero current point where the load current is positive going.

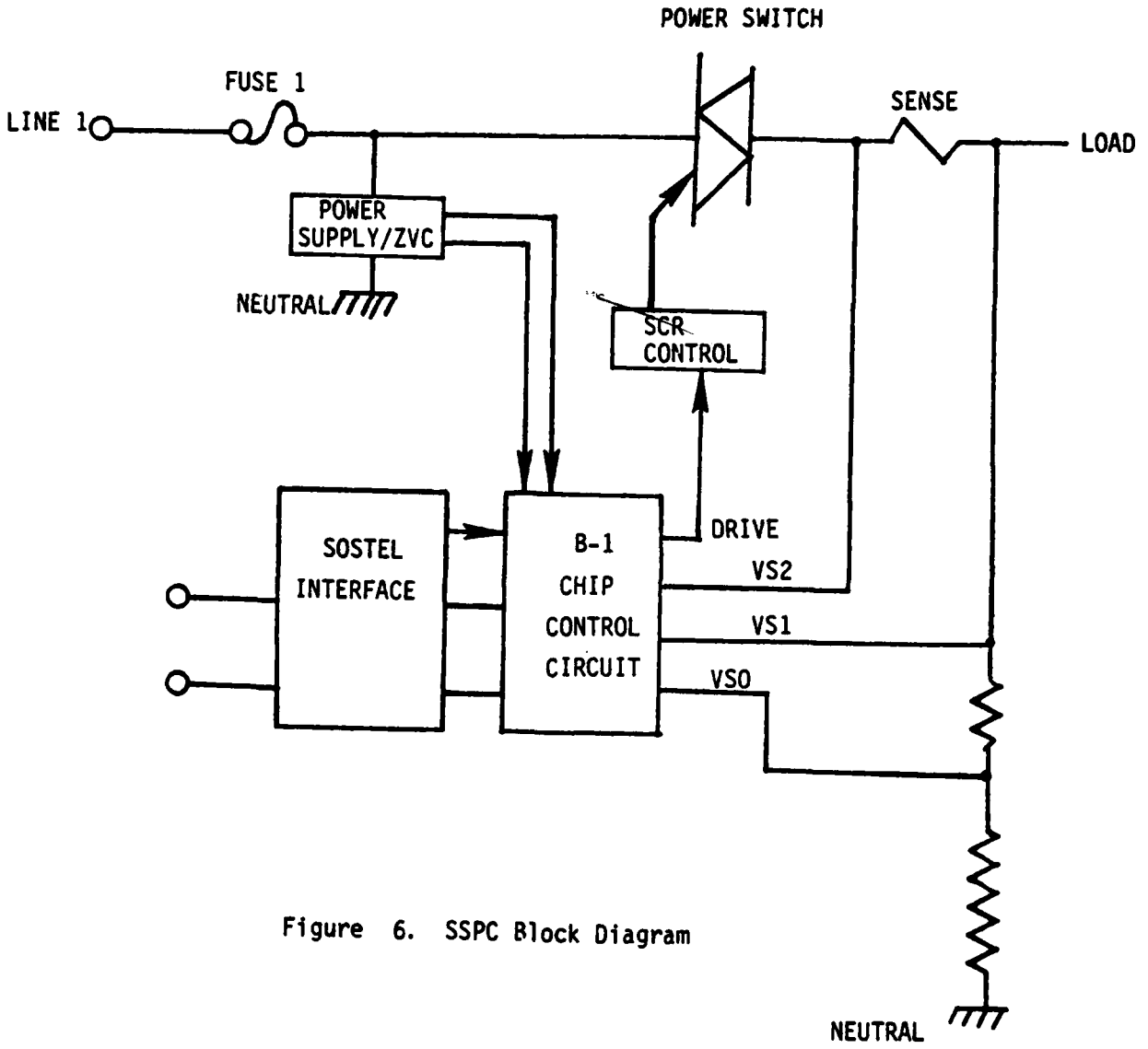


Figure 6. SSPC Block Diagram

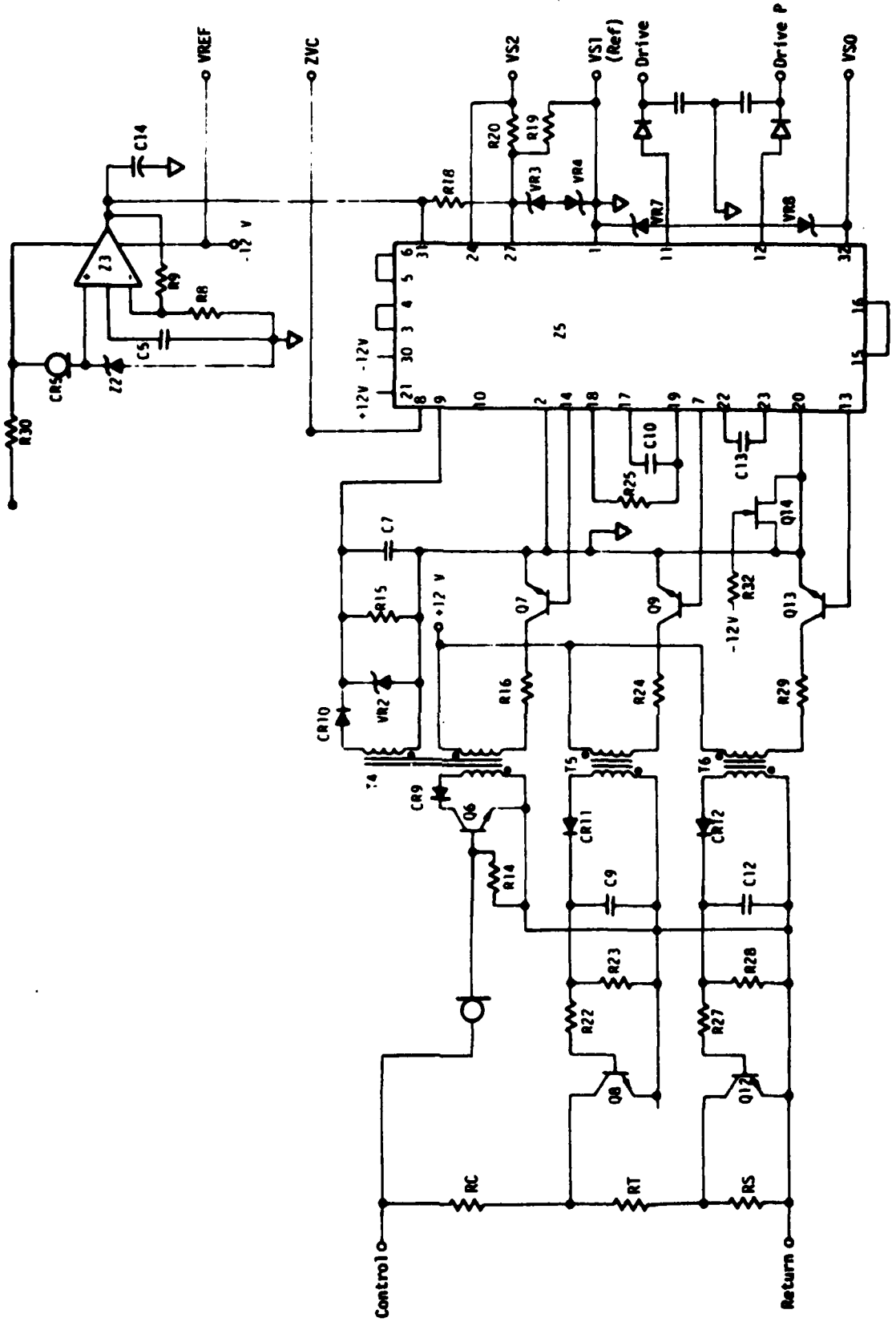


Figure 7. Control Circuit Schematic

3.2.2 Monolithic (continued)

Additionally, the monolithic device contains circuitry applying the ac voltage to the load; interface circuitry control input and outputs; and current sensing and trip timing logic for performing the general functions of load current sensing and trip timing computation. These functions are digitally implemented on the monolithic device.

The "sense" resistor (external to the monolithic) determines the quiescent (steady state) rating of the controller. The overcurrent protection slope is fixed by the trip algorithm of the monolithic. Figure 8 shows a plot of this algorithm together with the limits of NADC-30-TS-7602 and recommended trip limits. The vertical limit is the let-through current during and up to half-cycle shutdown of the SCR's during high current fault.

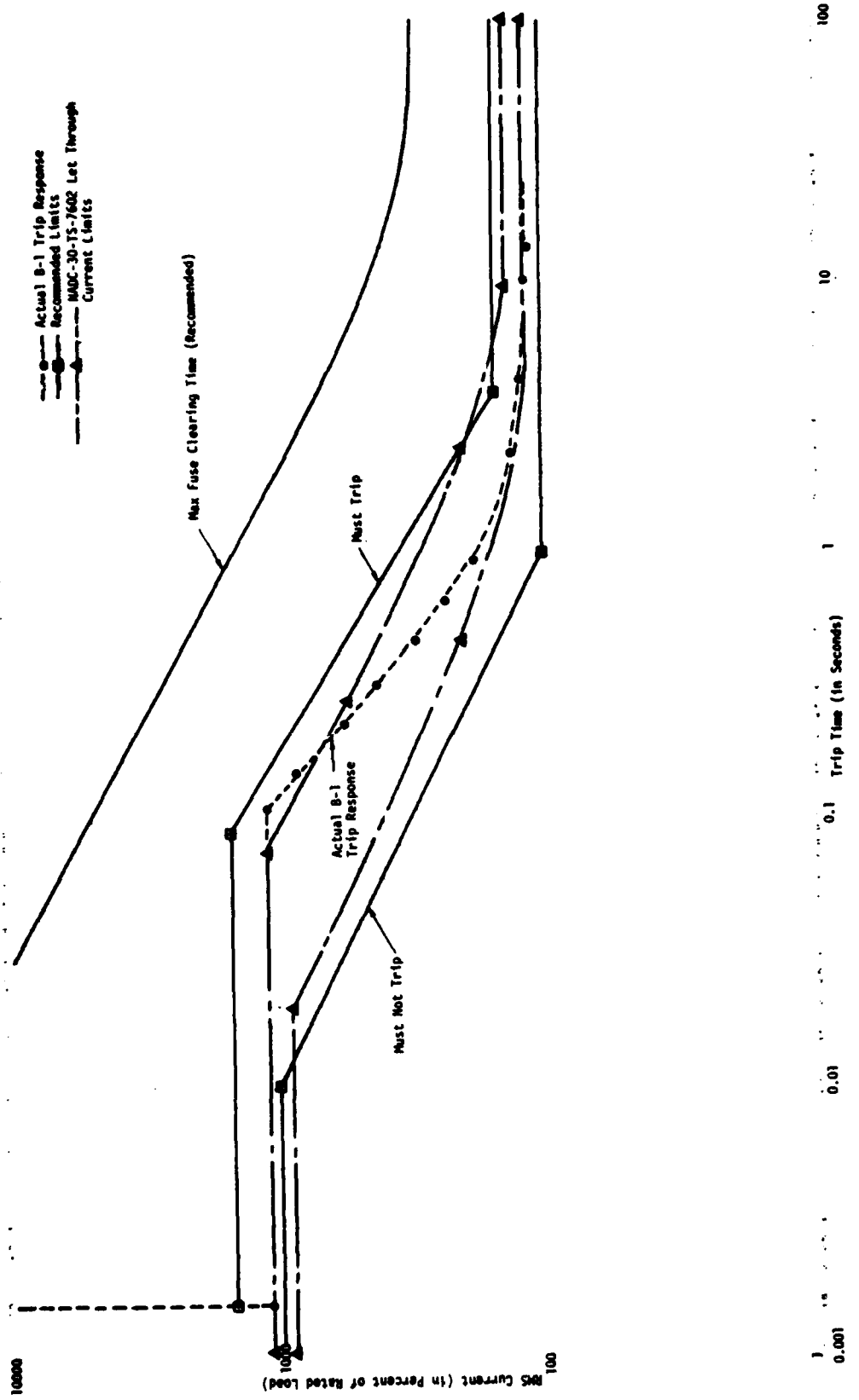


Figure 8. Recommended Trip Characteristics

3.2.3 SOSTEL Control and Monitoring. The SOSTEL System employs a bi-directional impedance change interface. A technique for transforming the B-1 SSPC interface to be SOSTEL compatible is shown in Figure 7 as a re-mechanization of the B-1 interface retaining transformer isolation.

With a 10 mA signal received at the control input for 5 msec, the SSPC is turned on, changing the input impedance to 720 ohms. If trip is issued by the monolithic, the output transistor is saturated, changing the input impedance to 420 ohms. For a fault/off condition, the status output is open, allowing the input impedance to rise to 1.1K ohms.

In the B-1 fault detection system, a shorted switch element is detected by determining that voltage is applied to the load (Status ON) without a proper control input command. Also less than 10% rated current would require a major change to the 'hard-wired' monolithic. The monolithic measures load current. However, a comparator plus logic would have to be added to output a signal when the rated current is less than 10% of rated. Thus, a complete SOSTEL interface is not achievable without additional changes to the B-1 SSPC.

3.2.4 Power Switch. The power circuit is shown in schematic form in Figure 9. The circuit performs the ac switching function and is used to apply power to a load. The circuit consists of two high voltage, medium current SCR's, associated SCR control circuits, and an RC snubber network.

The two SCR's are connected in an inverse parallel, i.e., back-to-back configuration. When gated ON, the SCR's will conduct, passing a current to the load.

The Resistive-Capacitive (RC) network consisting of RS and CS (see Figure 9) is used as a snubber circuit which is connected in shunt with the SCR's. The snubber network is used to reduce the rate of voltage rise across the switch in the event of a power line transient, thus preventing inadvertent turn on of the SCR's. With the SCR's off, the RC network will have line voltage impressed across it.

3.2.5 Power Supply. A pulse-width-modulated power supply converts the line voltage to ±12 Vdc. The ±12 Vdc is used to: (1) generate the +9 V reference power supply and (2) supply power to the monolithic. A preliminary schematic for the power supply is shown in Figure 10. This supply was developed by ASSD on IR&D in 1979.

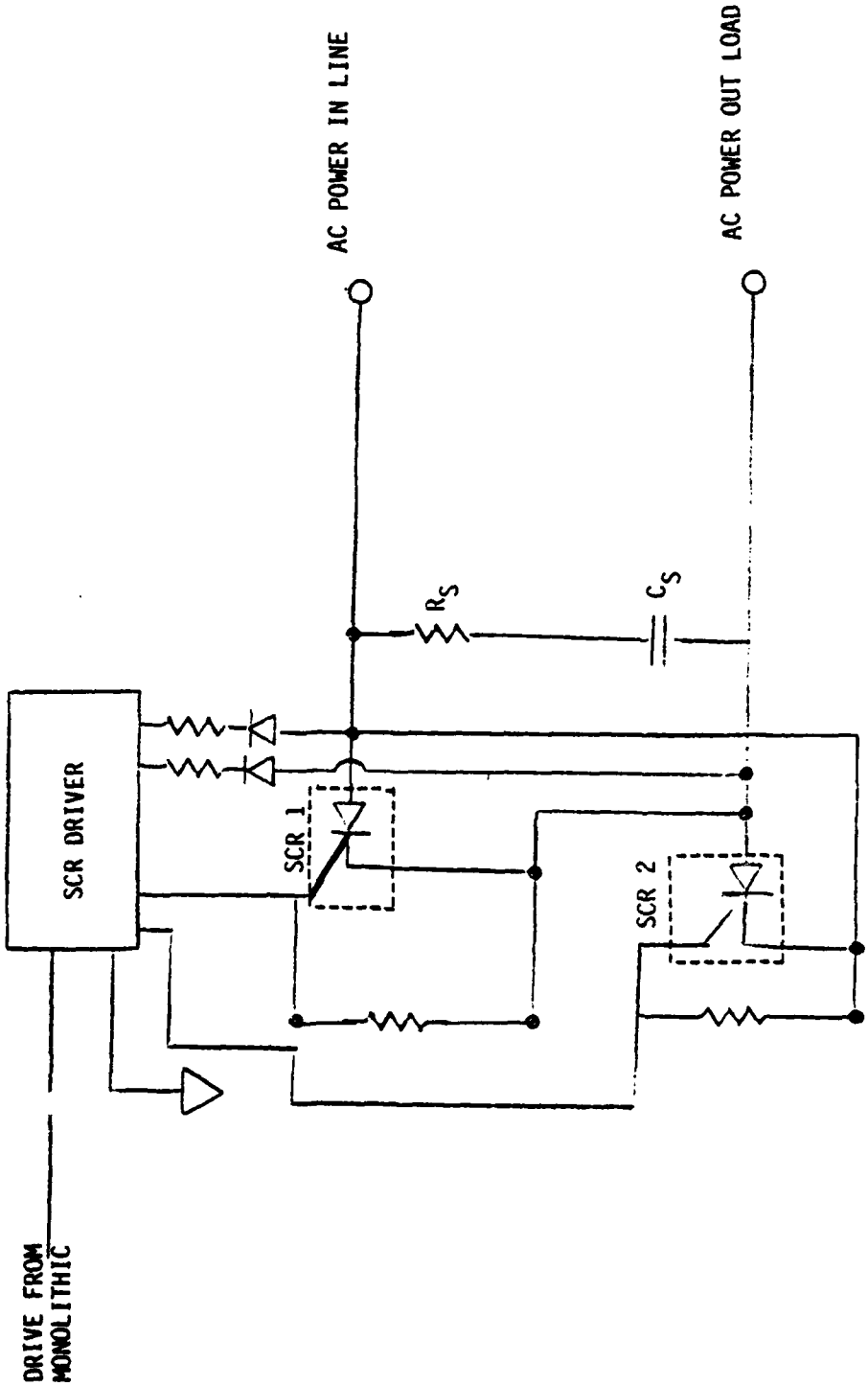


Figure 9. Power Switch Schematic

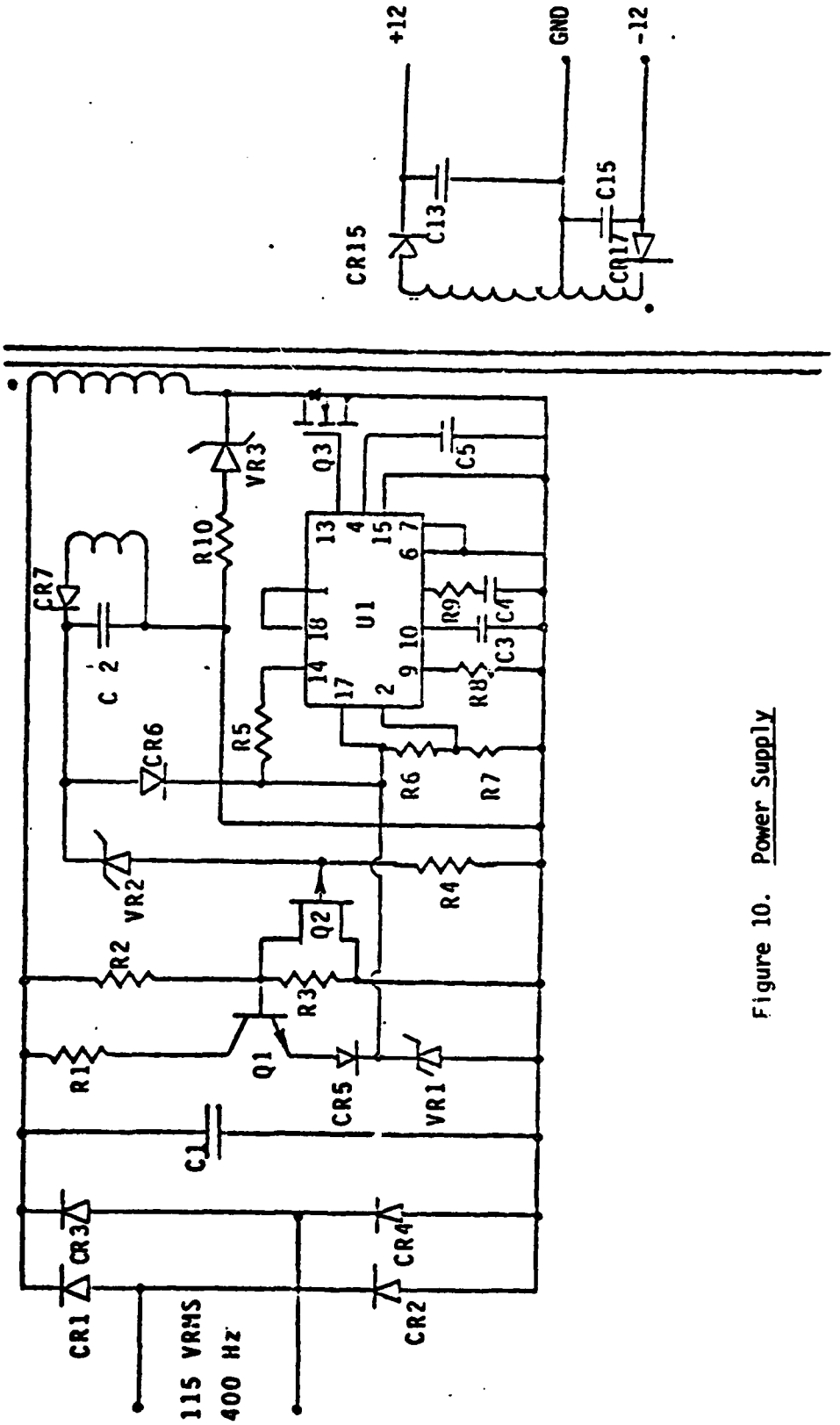


Figure 10. Power Supply

3.2.6 Zero Voltage Crossing. A zero voltage crossing (ZVC) detection circuit is shown in the schematic of Figure 11. Opto-coupling is used to provide isolation between the line and the internal circuitry that is referenced to the load. Its function is to generate 400 pps in synchronization with the zero crossing of the 115 Vac 400 Hz line. The pulses are used to turn on the SSPC at zero line voltage.

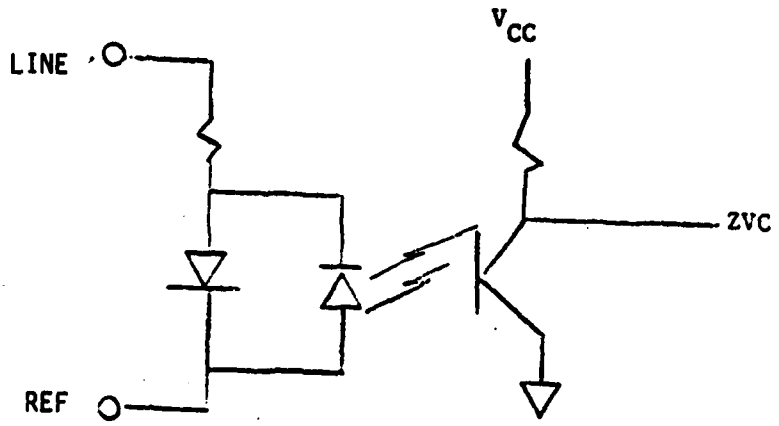


Figure 11. Zero Voltage Crossing Detection Circuit Schematic

3.2.7 Mechanization Summary. This mechanization described will satisfy the AAES functional requirements within the limitations of the monolithic device. The limiations are discussed in the specification section, 3.5. The preliminary mechanization and packaging study indicate that the envelope requirements will also be met. The packaging is discussed in the next section.

The monolithic, as mechanized, requires fabrication using a high voltage metal gate process, no longer active at Rockwell. To fabricate additional devices using this process requires reinstating the process. Rockwell's Microelectronics Device Division recommends the silicon gate process in lieu of the metal gate, primarily based on yield (lower cost) due to the lower voltage requirements. The silicon gate process requires a relayout of the monolithic device.

For prototype evaluation (small quantity), alternate control mechanizations should be considered.

3.3 Packaging

3.3.1 Circuit Apportionment. The AAES power controller, Figure 12, contains three microcircuits identified as Control, Power Supply, and Power Switch. The functions contained on these microcircuits were apportioned to minimize interface wiring. The 'feed through' pins are used to retain the physical spacing between the microcircuits as well as primary power and control signal interconnecting.

3.3.2 Control Circuit. The control microcircuit, Figure 13, contains the components shown in Figure 7. It is the least populated of the three microcircuits. However, its interconnect requirements are the most severe. The power dissipation of this microcircuit is nil.

3.3.3 Power Supply. The power supply microcircuit, Figure 14, contains the power supply shown schematically in Figure 10. In the proposed mechanization, the only internal power required is for the monolithic and the SOSTEL interface circuitry. Like the control microcircuit, the power dissipated on this microcircuit is nil.

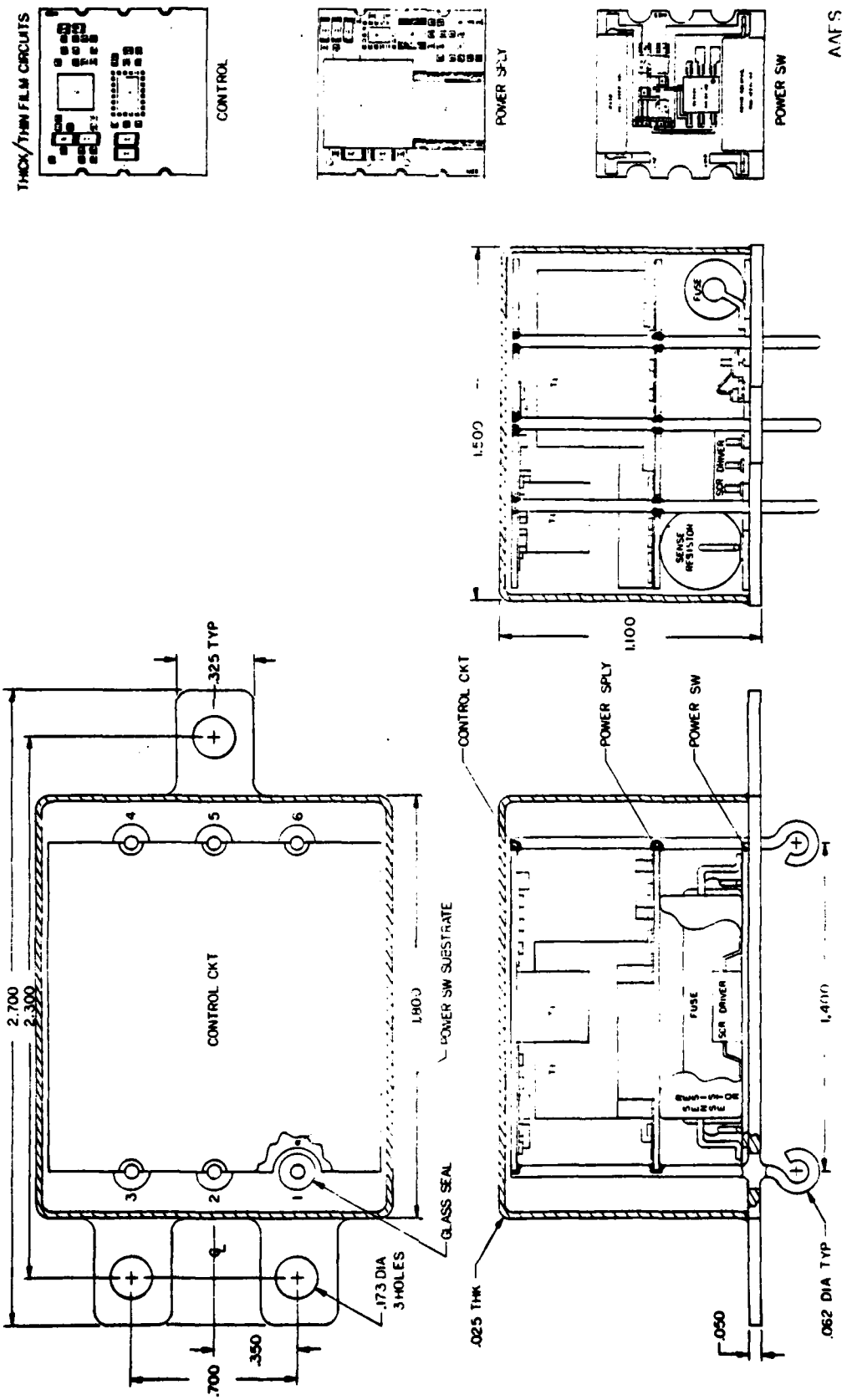


Figure 12. Hybrid Layout

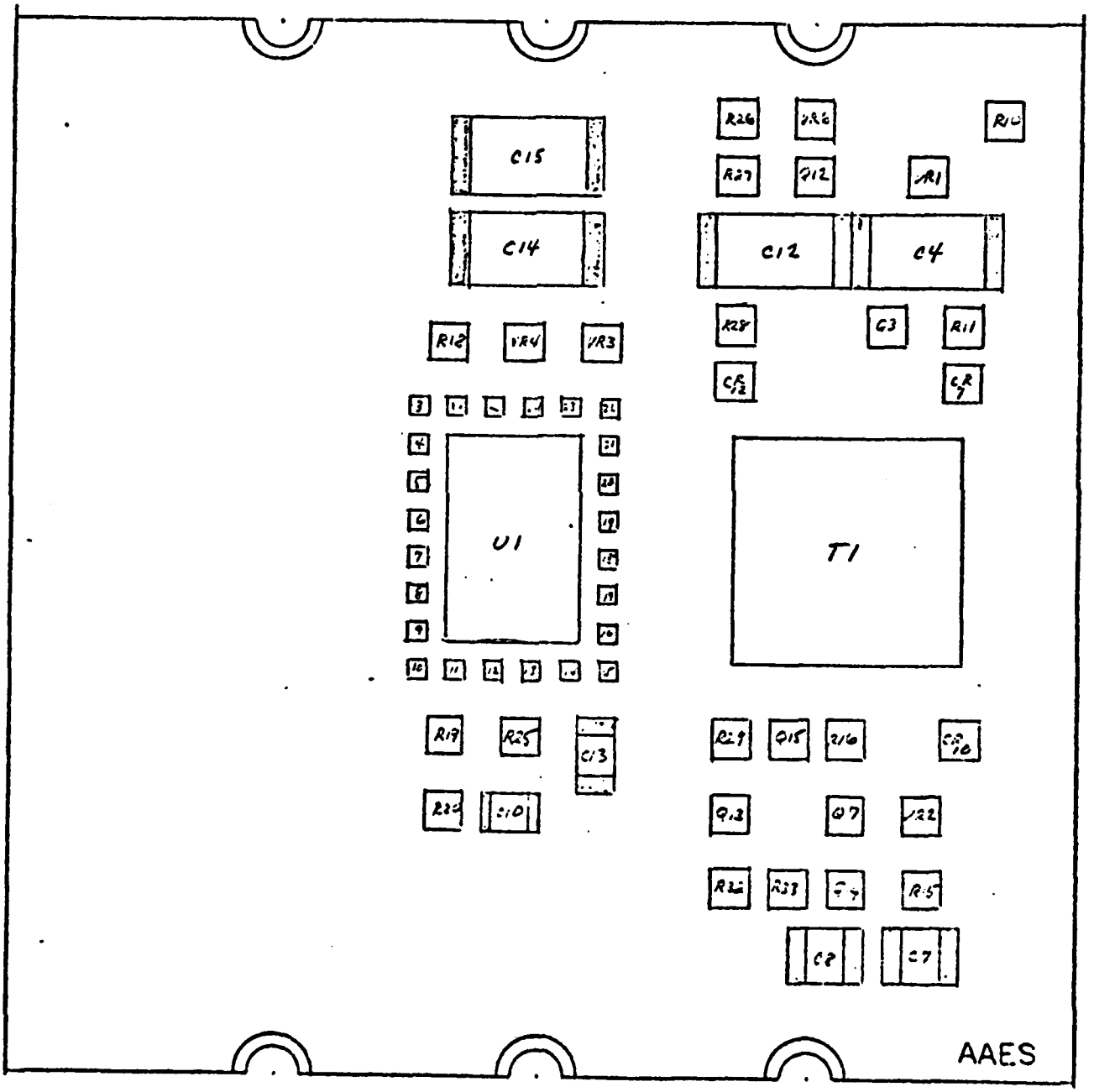


Figure 13. Control Microcircuit

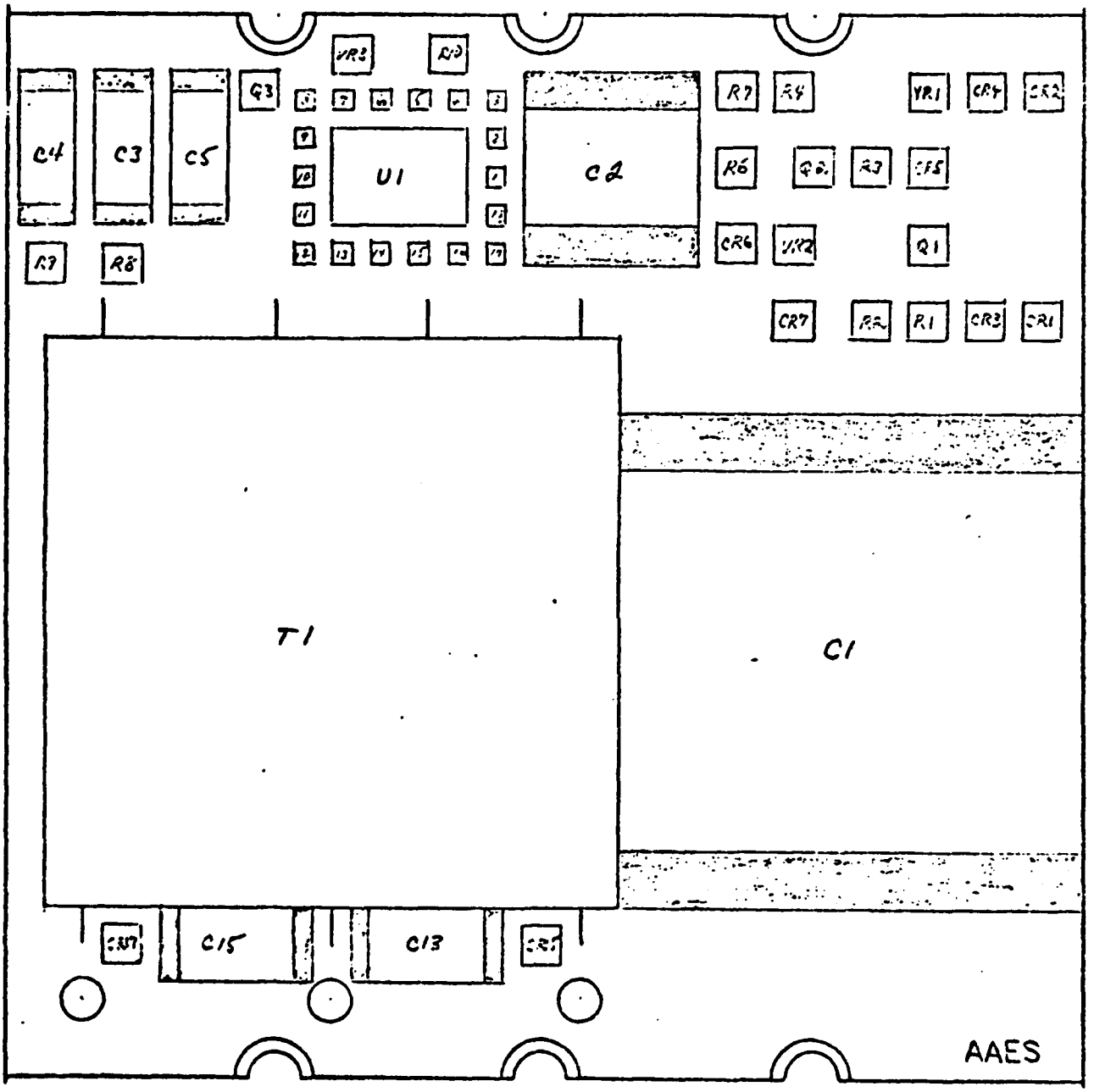


Figure 14. Power Supply Microcircuit

3.3.4 Power Switch. The power switch microcircuit, Figure 15, contains the series sense resistor, fuse, SCR switch and SCR drive circuitry. These are the major power dissipating components in the SSPC. The substrate material for the power switch is beryllia in lieu of the alumina for improved thermal characteristics. The SCR's are 'copper blocked', chip mounted directly to copper, to remove the heat from the junction. A copper alloy was selected for the SSPC base material to rapidly spread the heat away from the SCR's.

3.3.5 Thermal Analysis. A thermal analysis was performed for the 5 amp, the highest power dissipation configuration to determine the maximum allowable ambient temperature for continuous operation. A total power dissipation of 12 watts was assumed as the maximum worst-case condition.

The analysis was performed assuming 5 watts being dissipated in each SCR and 2 watts dissipated in the sense resistor. The substrate material for the power switch was 0.032 inch thick Beryllia 99.5 mounted on a .075" thick copper baseplate. Heat removal was via the three mounting tabs through the hold-down screws into the cold plate.

Heat removal, other than by direct conduction to the baseplate and mounting screws, such as radiated from the housing, was not used in the analysis and would provide some additional cooling paths.

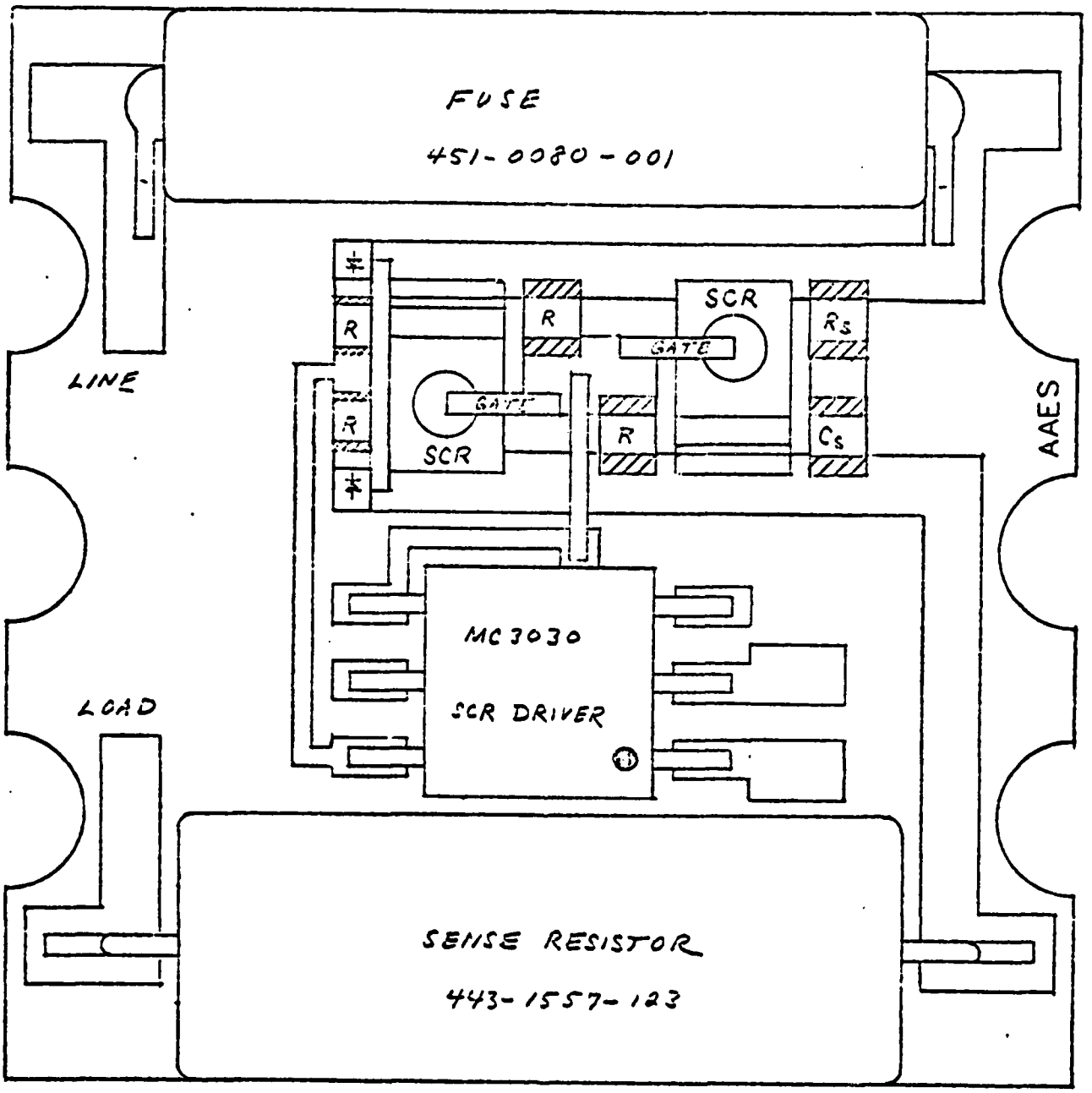


Figure 15. Power Switch Microcircuit

3.3.5 Thermal Analysis (continued)

With the above conditions, the temperature rise from baseplate ambient to the SCR junctions was 28.1°C. The SCR junction temperature limit is 125°C, so the maximum allowable ambient temperature limit (air and mounting panel) would be 96.9°C (206.4°F).

An increase in surface contact between the SSPC and baseplate that allows heat dissipation directly to the 'cold plate' and the addition of a pliable thermal material, such as chotherm, would reduce the thermal rise to half, i.e. approximately 14°C and increases the maximum allowable heat sink temperature to 111°C. Operation at 116°C or higher requires the selection of switch components other than SCR's.

The specification requirements of a thermal resistance equal to or less than 0.5°C/watt mounted dry to a 63 micro-inch or less mounting surface may be attainable but needs to be confirmed and would require tight control of installation conditions.

Again the analysis was based on worst-case conditions for the highest rated (5 amp) SSPC functioning at its full rating. It is suggested that the proposed packaging techniques will satisfy the vast majority of the AAES requirements and should be used with special installation considerations given to SSPC's with high ampere ratings.

3.3.6 Case. In the packaging studies, emphasis was placed on the selection of thermally compatible materials. The base material required the use of copper for thermal transmissibility. A hard copper alloy, tellurium copper, was selected for rigidity and compatibility with feed-through hermeticity requirements.

The feed-through, Figure 16, has a Kovar insert, glass seal, and Kovar feed-through. The design was reviewed by Tekform, Inc., to assure producibility. The housing (can) may either be soldered or brazed to the base. The internal SSPC atmosphere is then purged and sealed containing one atmosphere of dry nitrogen.

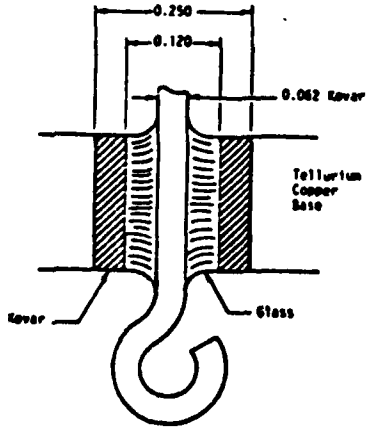


Figure 16. Feed-through Pin

3.3.7 Package Summary

The SSPC elements may be housed in the specified, i.e., 1.5" X 1.5" X 1.1" envelope. However, an 'allowed' envelope, 1.5" X 1.8" X 1.1", was used to enhance producibility and thermal transmissibility.

To provide the necessary mechanical stability, the second and third tier microcircuit substrates are secured to the baseplate via the terminals. The top of the terminals are threaded and the substrates are separated by insulated spacers. The assembly of substrates and spacers is then compressed against the baseplate by tightening nuts on the threaded ends of the terminals. This arrangement is expected to withstand the specified shock, vibration and acceleration environment.

The power controller packages will be hermetically sealed and are therefore expected to pass the specified salt, fog and humidity tests.

The weight of the package is estimated to be as follows:

• Power Switch substrate	0.4 oz.
• Power Supply microcircuit	0.8 oz.
• Control microcircuit	0.4 oz.
• Baseplate, terminals and housing	2.4 oz.
Total Package Weight:	4.0 oz.

3.4 SSPC Rating

The study effort included an evaluation of the applicability of the B-1 pass elements to satisfy AAES power controllers with the following ratings:

Part Number	Current (Amp)	Voltage (Vac)
TS7602/03A-001	0.5	115
TS7602/03A-002	2.0	115
TS7602/03A-003	5.0	115
TS7602/05A-001	1.0	26

The B-1 pass elements (SCR's) were purchased from Unitrode. They were 'selected' parts to an ASSD Procurement Specification, IID 479-1329-001. It can be used for the above AAES requirements. However, some of the controlled parameters that made the B-1 SCR's difficult to produce (and expensive) are not required for 115 Vac SSPC's, especially the high voltage rating (B-1 was double voltage).

The packaging configuration for AAES assumes using the same assembly technique as B-1 with a new SCR layout. Forty-five amp SCR's would still be used; however, the voltage rating would be reduced to a 300 to 400 V.

The 26 V SSPC requires a modification of the 115 V power supply to accommodate the input voltage differences. Other than 26 V changes, the designs are identical. The individual ratings are achieved with the selection of the appropriate sense resistor and fuse.

3.5 Specification

The requirements of Specification No. NADC-30-TS-7602 of 27 April 1976, with updates, were compared to the specification for the B-1 SSPC, Appendix A. The functional differences between these two specifications are summarized in Table I. These differences are discussed in the following paragraphs. The B-1 parameters are for the 230 Vac SSPC.

3.5.1 Life. The operating life (6×10^5) is that for a single SSPC, i.e one-fourth the B-1 module. The B-1 module is based on a reliability prediction in the B-1 environment. Special screens, over and above the B-1 controls, would be required to achieve the 10^6 life.

3.5.2 Power Dissipation. The no-load power is based on the internal power consumption. With the proposed mechanization, the 2.25 watts will be less. The new dissipation has not been established, but is estimated to be less than 1 watt.

3.5.3 Voltage Drop. The voltage drop across the SSPC under load is determined by the resistance of the fuse, shunt, and SCR's. A reduction of the voltage drop to $\approx$1.5V can be achieved by a redesign of the current sense circuit in the monolithic.

TABLE I. SPECIFICATION COMPARISONS

	115 Vac	26 Vac	230 Vac (1)
GENERAL			
Life	10^6	10^6	6×10^5
Leakage Current	2 ma	2 ma	2 ma at 75°C
Power Dissipation - Off	0.450 W	0.45	2.25 W
Common Mode	Applicable	Applicable	(New)
POWER CIRCUIT			
Voltage Drop			
No Load	3.2V/2.3V	1.5V rms	1.5V
Full Load	Same	Same	2.2V
Rupture Capacity	Unlimited	400A	400A
DC Offset			
No Load	(Nothing)	0.05V max	1V
Load			0.2V, 0.2A to 2.0A
Response			
Turn-on Time	1.5 msec max	2.75 msec	10 msec max
Rise Time	100V/µsec max 10V/µsec min		Not Applicable
Turn-off Time	2.0 msec max	2.75 msec	10 msec max
Fall Time	100V/µsec max 1.0V/µsec min		Not Applicable
Turn-on Delay	0.1 msec min 1.0 msec max	0.1 msec min 1.0 msec max	(5 msec built-in delay)
Trip Time	- See Figure -		
Zero Voltage Turn-on	±6V	±6V	±32V max
Zero Current Turn-off	$L_R \times 10^{-2}$ max	$L_R \times 10^{-2}$	±50 ma
CONTROL CIRCUIT			
SOSTEL Interface	Applicable	Applicable	New
Removal Time to Reset	5 msec min 20 msec max	5 msec min 20 msec max	5 msec min
Temperature Operating	-54 to +120°C	-54 +120°C	-55 to +71°C
Altitude	100,000 feet	100,000 feet	70,000 feet

(1) B-1 Modular Packaged SSPC Requirements

3.5.4 Rupture Capacity. The rupture capacity of the SSPC is determined by the ability of the wiring, fuse, shunt and SCR's to withstand a half-cycle short. The SCR's in this mechanization are steady state rated at 45 amps with a surge rating of 450 amps, thus the recommended limit of 400 amps for all controllers.

3.5.5 DC Offset. The dc offset can be controlled by screening (selecting) SCR's for matched pairs, a costly process if the usage does not require tight control.

3.5.6 Response. The B-1 monolithic has a 5 millisecond fixed delay, then waits for the next positive going zero voltage crossing, allowing up to 2.5 ms of additional delay. The delay is the same for turn on and turn off. The same holds true for turn off current to achieve full cycle control.

3.5.7 Trip Time. Figure 7 is a plot of the specified trip curve, the monolithic capability and recommended trip limits. SCR's require a zero current crossing to turn off, therefore a peak let through of input terminal power capability will be 'let through current' for 1.25 milliseconds maximum (one-half cycle of 400 Hz).

3.5.8 Zero Voltage Turn on, Zero Current Turn off.

The B-1 SSPC, when scaled for 115 Vac, is within ±10 V of zero crossing. The proposed design uses a Motorola 3030, or equivalent, which should be within ±6 volts.

The zero current turn off is a function of the rated load and the SCR characteristics. For the SCR's used, the current is ±50 ma or 5% of rated load, whichever is greater.

3.5.9 Control Circuit. The control input proposed adopts the B-1 SSPC to a SOSTEL compatible interface in the following manner:

The B-1 monolithic 'status' detects (1) there is voltage to the load, and (2) that the SCR's are not half-waving. If these two conditions are met, a valid status results, i.e. 'no fault'. The 'trip' output provides an overcurrent indication. These signals are applied as switches in the SOSTEL interface adaptation. A Fault/OFF is defined as a 1.1K ohm impedance and an overcurrent trip of 420 ohms. Normal operation is 720 ohms. The test condition of 4.8.7.29 (b) and (c) can be met with the proposed configuration. Condition (a) requires current monitoring not presently mechanized in the monolithic.

3.5.10 Removal Time to Reset. Refer to Paragraph 3.5.6 for delay time comments. The reset of the SSPC is accomplished by removing control and reapplying it. Other than the built-in delay, it is externally controlled.

3.5.11 Temperature.

The maximum operating junction temperature for SCR's is 125^{o}C. Beyond that gate control is lost, i.e. cannot turn SCR's off. From a reliability standpoint, this temperature (125^{o}C) should be derated. It is recommended, therefore, that the maximum SSPC baseplate temperature be maintained at 80^{o}C or less for reliability considerations.

3.6 Reliability Prediction

3.6.1 AAES Configured SSPC. A summary of the reliability prediction on the Power Controller as presented below was derived by modifying the original prediction performed for the B-1 Program. The control and power substrate failure rates were used by removing the components no longer used and by adding a new IC (driver) on the power substrate. A new substrate was predicted for the power supply using components taken from the old control module.

Since the B-1 prediction was used to make this prediction, the failure rates and ground rules are to MIL-HDBK-217B which was current at the time of the B-1. The environmental conditions assumed were aircraft controlled environment (Airborne Inhabited). The thermal conditions are as indicated in the table.

AAES CONFIGURED SSPC RELIABILITY PREDICTION

Baseplate Temperature	Package Mounting	Temperature Highest Junction	Failures Per Million Hours	Equivalent MTBF (Hrs)
25°C	Full Base	40°C	2.5954	385297
25°C	Tab Only	55°C	4.3778	228420
80°C	Full Base	95°C	15.9477	62704
80°C	Tab Only	110°C	23.7652	42087

3.6.2 B-1 SSPC Reliability Prediction. The following sections presents the B-1 Aircraft SSPC reliability prediction. The prediction is then modified for the changes required for the AAES SSPC configuration. The modifications are indicated by crossing out and substituting AAES numbers or by noting the item with an "AAES".

3.6.2.1 General. This reliability prediction has been prepared in accordance with MIL-STD-756, Reliability Prediction Methods. All failure rates and failure rate models are taken directly from MIL-HDBK-217B. A unique model was developed for the monolithic as discussed in Paragraph 3.6.2.2 (8).

3.6.2.2 Prediction Ground Rules - B1 SSPC. The SSPC reliability prediction is based on the following set of ground rules:

(1) All failure rates are considered constant and are within their useful life period.
(2) The infant mortality period has been expired through hybrid burn-in.
(3) The failure distribution is assumed to be exponential.
(4) The environment used is aircraft inhabited.
(5) Component quality levels are:
    (a) MIL-M-38510 Class B for all IC's and hybrids.
    (b) JANTX for all semiconductors.
    (c) MIL established reliability level "M" for all resistors and capacitors (discrete).
(6) Temperature used for the prediction was $60^{o}C$ for the highest temperature within a hybrid package.
(7) The following factors are obtained from MIL-HDBK-217B for microcircuits:

λ_b = Basic failure rate in failures per million hours.

$$\lambda_b = \lambda_s + A_s\lambda_c + \Sigma\lambda_{RT}N_{RT} + \Sigma\lambda_{DC}\,N_{DC} + \lambda_{PF}\,\pi_{PF}$$

where:

λ_S = Substrate contribution
A_S = Substrate area in square inches
λ_C = Network complexity
λ_{RT} = Failure rate of resistors
N_{RT} = Number of resistors
λ_{DC} = Failure rate of discrete chips
N_{DC} = Number of discrete chips
λ_{PF} = Failure rate for package factor
π_{PF} = Package adjustment factor

λ_P = Device failure rate in failures per million hours.

$\lambda_P = \lambda_b (\pi_{T_2} \times \pi_E \times \pi_F \pi_Q)$

where:

π_{T_2} = Temperature factor

π_E = Environment (airborne inhabited)

π_F = Circuit function factor

π_Q = Quality level = 1 (Class B)

(8) The Monolithic CMOS/SOS chip failure rate for the digital section was predicted using the expression:

$$\Gamma_D = \pi_Q (C_1 \pi_T + C_2 \pi_E) \pi_p$$

where:

$C_1 = 5.384\ 10^{-4} NG^{0.779}$

$C_2 = 5.240\ 10^{-4} NG^{0.7}$

NG = Number of $\frac{\text{FETS}}{4} = \frac{3040}{4}$

π_Q, π_T, π_E and π_p are all from MIL-HDBK-217B.

3.6.2.3 Reliability Prediction Worksheets

The B-1 SSPC Reliability Prediction worksheets for the control, power and power supply microcircuits, modified for AAES, are presented in the following sections.

3.6.2.3.1 Control Microcircuit Reliability Prediction Worksheet

	Qty.	F/R	π	Total
Transistor 02 (NPN)	~~11~~ 5	.0053	.2	.01166
(PNP)	~~2~~ 1	.0077	.2	.0030
Diode (Logic)	~~13~~ 5	.0048	.2	.01248
(Zener)	~~2~~ 5	.022	.2	.0083
Capacitor (CER)	~~13~~ 6	.0004		.0052
(THNT)	~~1~~ 2	.004		.0040
Transformer	~~3~~ 2	.0002		.0006
IC's				
CMOS/SOS 760G/114L	1	.1493	1.0	.1493
LM113 (DIG)	~~2~~	.0167	1.0	.0334
LM105 (18Q LIN)	~~1~~	.0249	2.0	.0498
LM108 (29Q LIN)	~~1~~	.0334	2.0	.0668
Resistors (AAES)	13			
				~~.34504~~
		$\Sigma\lambda_{DC}N_{DC}$		0.3283

$$\lambda_b = \lambda_S + A_S\lambda_C + \Sigma\lambda_{RT}H_{RT} + \Sigma\lambda_{DC}N_{DC} + \lambda_{PF}\pi_{PF}$$

λ_S = .02

$A_S\lambda_C$ = .8 X 1.3 X .006 = .00624

$N_E = N_{LT} + N_{2T} + N_{DC} = (147 \times 2) + 31 + 54 = 379$

NE/AS = 379/1.04 = 365 λ_C = .006

$\pi_{PF} \cdot \lambda_{RT}$ = 3.3 X .01 = .033

$\Sigma\lambda_{RT}N_{RT}$ = 21 X .0005 + 10 X .00012 = .0117

λ_b = .02 + .00624 + .0117 + .34504 + .033 = .41598

AAES λ_b = .02 + .00624 + .0065 + .3283 + .033 = .39404

B-1 $\lambda_p = \lambda_b (\pi_T \times \pi_E \times \pi_F)$ = .41598 (1.7 X 4.0 X 1.0 X 1.1) = 3.1115

3.6.2.3.2 Power Microcircuit Reliability Prediction Worksheet

	QTY.		F/R		Total
Diode (Logic)	~~6~~	2	.0048	.2	.00576
(S/S)	~~4~~		.0081	.2	.00648
Capacitor	~~7~~	1	.0004	-	.0028
J - FET	~~2~~		.021	.2	.0084
SCR	2		.050	.2	.020
IC (AAES)	1		.046		~~.04344~~
R_{FUSE} (AAES)	1		.10		
R_{SENSE} (AAES)	1		.066		
					.106

$\lambda_b = \lambda_S + A_S\lambda_C + \Sigma\lambda_{RT}N_{2T} + \Sigma\lambda_{DC}N_{DC} + \lambda_{PF}\pi_{PF}$

$\lambda_S = .02$ $\quad \lambda_{PF}\pi_{PF} = 2 \times .01 = .02$

$N_E = N_{LT} + N_{RT} + N_{DC}$ = (LOGIC) = 42 + 7 + 19 = 68

(PWR) = 10 + 0 + 2 = 12

NE/AS = 68/(1.2 X 1.2 - .67 X .67) = 68 (LOGIC)

= 12/(.67 X .67) = 27 (PWR)

$A_S\lambda_C$ = (1.2 X 1.2 - .67 X .67) X .001 = .00099 (LOGIC)

(.67 X .67) .001 = .00045 (PWR)

$\Sigma\lambda_{RT}N_{RT}$ = 7 X .00012 = .00084 (LOGIC)

λ_b = .02 + (.00099 + .00045) + .00084 + .04344 + .02 = .08572

AAES λ_b = .02 + .00045 + .00072 + .106 + .02 = .14717

B-1 $\lambda_p = \lambda_b(\pi_{T2} \times \pi_E \times \pi_Q \times \pi_F)$ = .08572 (1.7 X 4.0 X .1 X .3 = .4663

3.6.2.3.3 Power Supply Microcircuit Reliability Prediction Worksheet (New for AAES)

	QTY.	F/R	
Capacitor (CER)	1	.0004	
(THNT)	6	.004	
Diode	11	.0048	
(Zener)	3	.022	
Transformer (NPN)	1	.0053	
(PNP)	2	.0077	
IC SG1526	1	.0167	
		$\Sigma\lambda_{DC}N_{DC}$	.1768

$$\lambda_b = \lambda_S + A_S\lambda_C + \Sigma\lambda_{RT}N_{RT} + \Sigma\lambda_{DC}N_{DC} + \lambda_{PF}\ \pi_{PF}$$

$$\lambda_b = .02 + .00624 + .0045 + .1768 + .033 = .24054$$

3.6.2.3.4 AAES SSPC Reliability Prediction Worksheet

$$\lambda_p = \lambda_b (\pi_{T2} \times \pi_E \times \pi_F \times \pi_Q)$$

$$\pi_E = 4,\ \pi_F = 1,\ \pi_Q = 1,\ \lambda_b = PS\lambda_b + C\lambda_b + P\lambda_b = .78175$$

Temperature Highest Junction	π_{T2}	λ_p	MTBF (Hours)
40°C	.83	2.5954	385,297
55°C	1.4	4.3778	228,420
95°C	5.1	15.9477	62,704
110°C	7.6	23.7652	42,087

IV. CONCLUSIONS AND RECOMMENDATIONS

4.1 Modular Packaging. For new aircraft, the integration of the Universal Terminal and SSPC's in the Load Management Center, using module packaging techniques, should be considered. The B-1 SSPC module can be readily modified for a SOSTEL interface, 115 V operation, and up to 5 amps, without changing the printed wiring. This packaging concept can be applied to the 28 Vdc and 270 Vdc SSPC's as well as the ac. The Control Hybrid could be configured to be standard for all requirements--28 Vdc, 270 Vdc, 115 Vac and 26 Vac.

4.2 Packaged SSPC. A SSPC can be configured to satisfy the envelope constraints of NADC-30-73-7602 using the B-1 monolithic and pass elements i.e. SCR's. The remainder of the B-1 SSPC circuits were replaced with recently developed configurations that either eliminate or considerably reduce the mass of components, especially transformers and filter capacitors.

4.3 B-1 Monolithic. The B-1 monolithic contains a fixed control delay, 5 millisecond and a fixed trip-time relationship. With these restrictions, the device can be adapted to the AAES requirements.

The B-1 monolithic was mechanized using a metal gate, high voltage nitrate process. This process has been replaced with silicon gate process at Rockwell. It is recommended that the B-1 monolithic be converted to the silicon gate process for future applications. The functional organization of the device should be reviewed for potential update along with the process conversion.

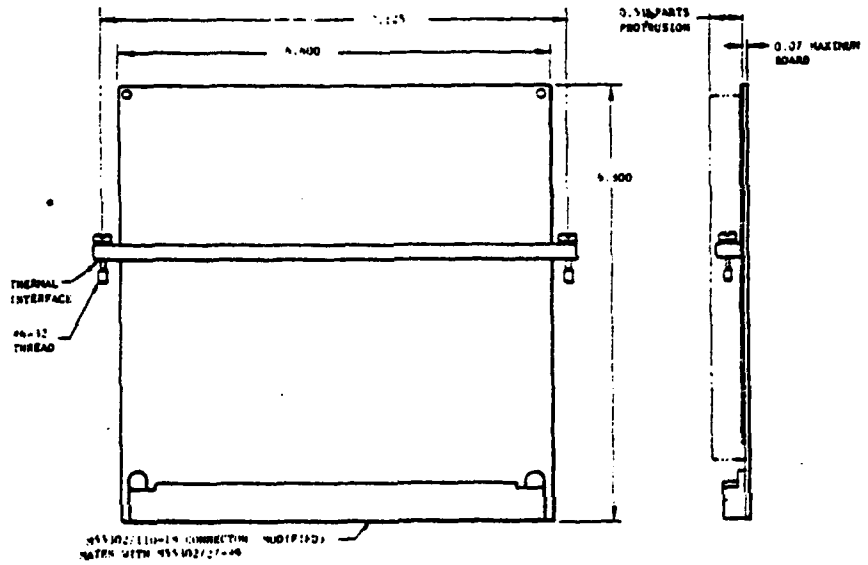
4.4 Thermal. The proposed package design will provide satisfactory performance for most applications. Special installation considerations should be given to the 5 amp rated SSPC to assure a good thermal path to the cold plate. The cold plate for 5 amp SSPC's should be maintained at 71°C or less for reliability considerations. The SCR junction temperature must not exceed 125°C for safe operation.

APPENDIX A

MIL-P-81653 (RECOMMENDED)
MILITARY SPECIFICATION SHEET

POWER CONTROLLER, AC LOAD SWITCHING
SPST, NORMALLY OPEN OR NORMALLY CLOSED 0 THRU 2 AMPERES

The complete requirements for procuring the controllers described herein shall consist of this document and the latest issue of MIL-P-81653.



1 AC OUTPUT B	29 B CONTROL IN	57 *	85 C TRIP
2 *	30 B CONTROL RETURN	58 *	86 B CONTROL RETURN
3 *	31 A TRIP	59 SPARE	87 B CONTROL IN
4 RECTIFIED AC -OUT B	32 S/T RETURN	60 *	88 B CITS STATUS
5 *	33 A STATUS	61 *	89 B STATUS
6 *	34 A CITS STATUS	62 SPARE	90 S/T RETURN
7 RECTIFIED AC -OUT B	35 A CONTROL IN	63 *	91 B TRIP
8 *	36 A CONTROL RETURN	64 *	92 AC INPUT NEUTRAL
9 *	37 SHIELD	65 SELECT IN C	93 *
10 AC OUTPUT C	38 *	66 *	94 *
11 *	39 *	67 *	95 RECTIFIED AC -OUT B
12 *	40 SPARE	68 RECTIFIED AC -OUT C	96 *
13 SPARE	41 *	69 *	97 *
14 *	42 *	70 *	98 RECTIFIED AC -OUT B
15 *	43 SPARE	71 RECTIFIED AC -OUT C	99 *
16 SPARE	44 *	72 *	100 *
17 *	45 *	73 *	101 AC SELECT IN
18 *	46 AC OUTPUT B	74 AC INPUT	102 *
19 AC INPUT	47 *	75 AC INPUT	103 *
20 AC INPUT	48 *	76 *	104 SPARE
21 *	49 RECTIFIED AC -OUT A	77 *	105 *
22 *	50 *	78 *	106 *
23 *	51 *	79 AC INPUT NEUTRAL	107 SPARE
24 SHIELD	52 RECTIFIED AC -OUT A	80 C CONTROL RETURN	108 *
25 B TRIP	53 *	81 C CONTROL IN	109 *
26 S/T RETURN	54 *	82 C CITS STATUS	110 AC SELECT IN
27 B STATUS	55 AC OUTPUT A	83 C STATUS	
28 B CITS STATUS	56 SELECT IN B	84 S/T RETURN	

*PINS REMOVED TO PROVIDE ISOLATION REQUIRED FOR 270V OPERATION.

REQUIREMENTS:

MECHANICAL AND DIMENSIONAL CHARACTERISTICS

Configuration	See Page 1
Dimensions	Inches
Tolerances	±0.03 for two place decimals
	±0.01 for three place decimals
Enclosure	Not applicable
Weight	1 lb
Mounting torque.....	Not applicable
Leak rate	Not applicable

THERMAL CHARACTERISTICS

Thermal resistance module mounting tab to	
heat exchanger	0.6°C/ W with
Heat exchanger temperature	70°C maximum

ELECTRICAL CHARACTERISTICS (-54 to

General

Circuit arrangement	SPST NO or NC (see Figure 1)
Insulation resistance	100 megohms minimum
Dielectric withstanding voltage:	
230 V lines	1300 V rms at sea level
	800 V rms at 70,000 ft
non-230 V lines	900 V rms at sea level
	200 V rms at 70,000 ft
Isolation	
Life (operating hours).....	125,000 minimum
Radio interference.....	applicable
Leakage current	2.0 mA at 75°C
Power dissipation	
'ON'.....	5.5 W at 2 A
'OFF'.....	2.25 W
Common mode rejection	±10 V peak, 1 Hz to 100 kHz

MIL-P-81653 (RECOMMENDED)

Power Circuit

Supply Voltage	
Steady state	see Figure 2
Transients (long term)	see Figure 2
Transients (short term)	see Figure 2
Current	
Rated (no load to 100% rated)	0-2 A 400 Hz
	0-200 mA DC
Frequency (rated)	400 Hz ± 5%
Voltage drop	
No load	1.5 V
100% load	2.2 V
Current limiting	
Ripple current	Not applicable
Rupture capacity	400 A
DC offset voltage:	
No load	1 V
Load	0.2 V, 0.2 A to 2.0 A
Overshoot current	Not applicable
Fail safe current	see Figure 3
Reset immunity	applicable

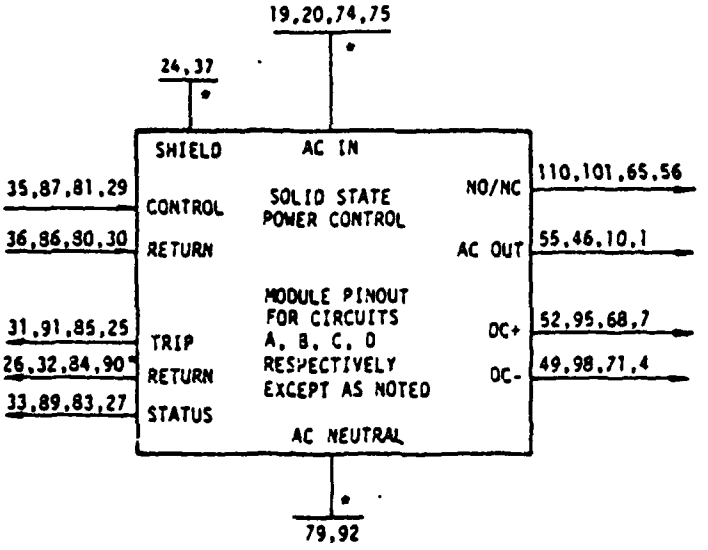
Transients:	
Operating voltage	10 msec maximum
Spike overvoltage	±510 Vdc
Standby power	±510 Vdc
Response:	
Turn-on time	10 msec maximum
Rise-time	Not applicable
Turn off time	10 msec maximum
Fall time	Not applicable
Trip free	applicable
Trip time	see Figure 3
Zero voltage turn-on	±32 V maximum
Zero voltage turn-off	±50 mA maximum

Control Circuit

Supply voltage	see Figure 4
Current	see Figure 4
Turn-on current	see Figure 4
Turn-off current	see Figure 4
Removal time to reset	4 msec minimum

Environmental Characteristics

Module Temperature	
Operating	-55°C to 71°C
Storage	-65°C to 150°C
Shock	
Mechanical	applicable
Temperature	applicable
Vibration	applicable
Acceleration	100 g
Salt fog	applicable
Humidity	applicable
Operation at temperature extremes	applicable
Temperature - altitude	applicable
Operating ambient:	
Temperature	-65 to 71°C
Altitude	Sea level to 70,000 ft



*COMMON for all four power controller circuits

Fig. 1. SSPC Input/Output Diagram

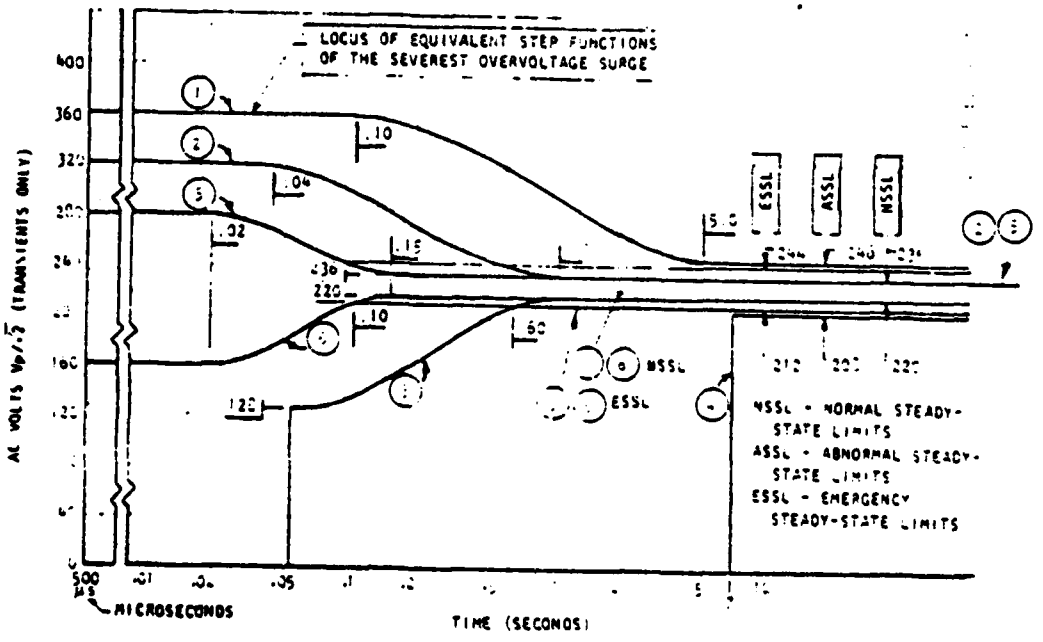


Fig. 2. Double Voltage AC Power, Transient Surge AC Voltage Step Function Loci Limits for Category A Equipment

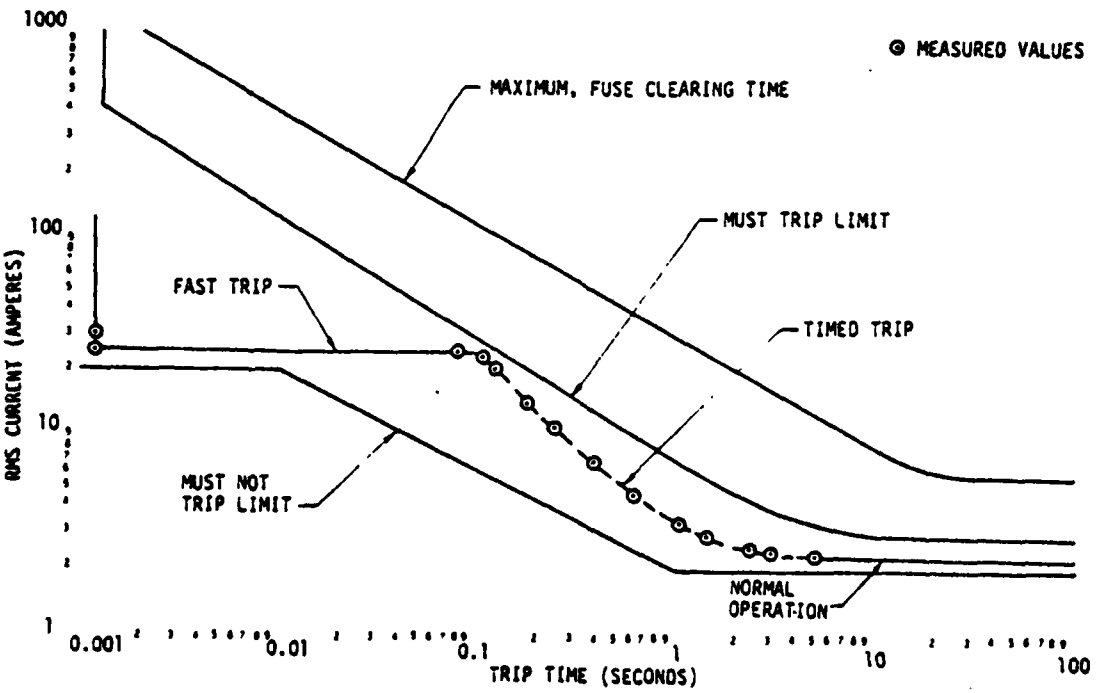


Fig 3. Timed Trip and Fuse Clearing Time Requirements

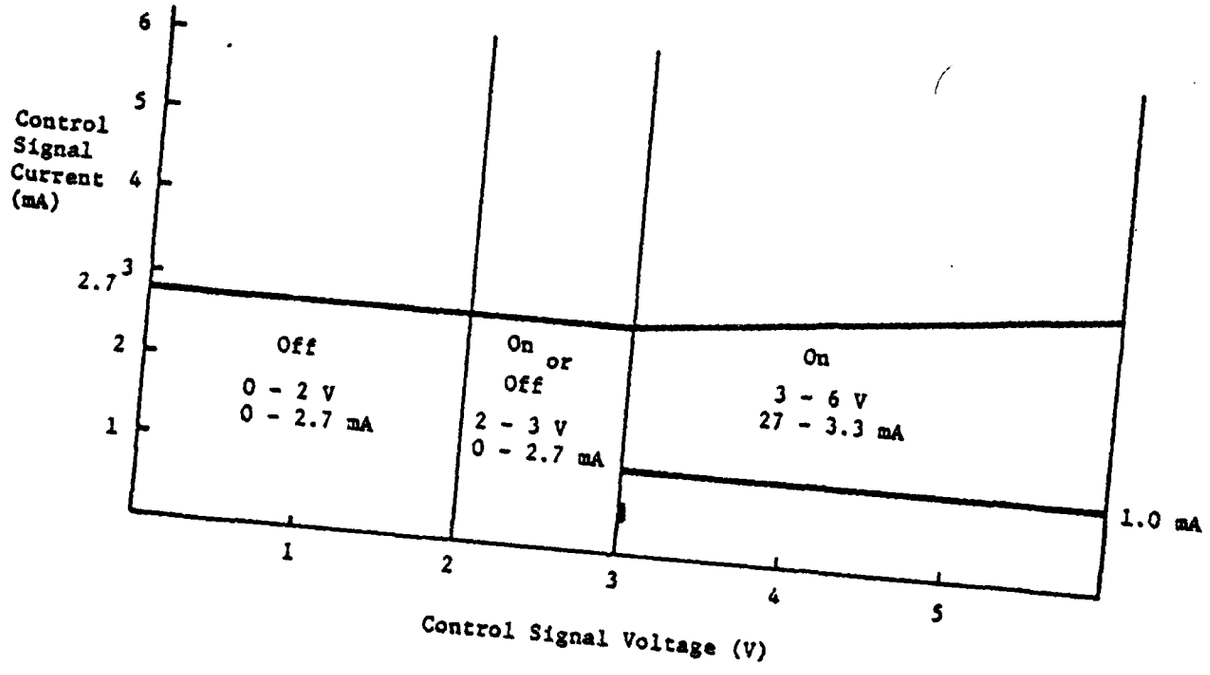


Fig.4. Turn-on/off Voltage Requirements

NADC 79134-60

A ROCKWELL CMOS/SOS/LSI SOLID-STATE POWER CONTROLLER CHIP

23 August 1979

Prepared By

W. A. McFall

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A ROCKWELL CMOS/SOS/LSI SOLID-STATE POWER CONTROLLER CHIP

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A ROCKWELL CMOS/SOS/LSI SOLID-STATE POWER CONTROLLER CHIP

W. A. McFall

Autonetics Strategic Systems
Anaheim, California

INTRODUCTION

The Solid-State Power Controller Monolithic Chip (Part Number 30351, Patent Pending) is a Complementary Symmetry Metal Oxide Semiconductor (CMOS) Silicon-on-Sapphire (SOS) Large Scale Integrated Circuit (LSI) that is intended for use as the control portion of a Solid-State Power Controller (SSPC). The chip contains, on a single monolithic device, the analog and digital circuitry to turn on, turn off, monitor resulting overloads, and to accomplish emergency shutdowns of the solid-state switches that are employed in solid-state power control.

This document describes the operation and sequencing internal to the monolithic to better enable a potential user to apply the device to his system in the most prudent manner.

Power Controller Functions

The primary purpose of a Solid-State Power Controller is to provide full cycle control while monitoring the magnitude of ac power being delivered to an electrical load. This full-cycle control is provided by driving a solid-state pass element, beginning with the line voltage zero crossing (ZVC) and ending with a completed cycle of the load current at zero-current crossing (ZIC) (see Figure 1).

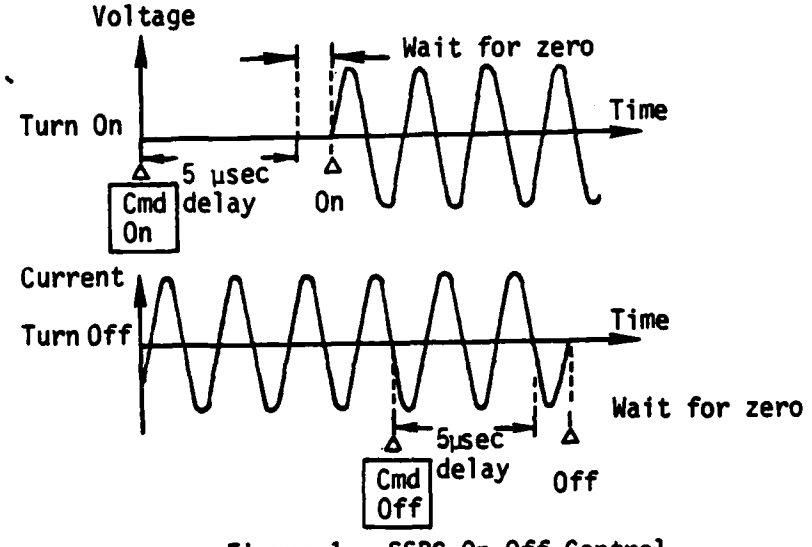


Figure 1. SSPC On-Off Control

While the solid-state pass element is "on", the Solid-State Power Controller monitors the load current through the pass element and computes a turn-off point (Trip Time) for every value of load current in excess of 110% of the rated current. When the load current exceeds the rated current by more than 110% for longer than the computed trip time, the drive to the solid-state pass elements is extinguished without regard to the load-current zero crossing (ZIC). A characteristic curve, Figure 2, shows the time allotted before trip or shutdown as a function of a load current. Full-cycle control is accomplished by timing the enabling and disabling of complementary DRIVE outputs through which the power switches, or pass elements, are turned on and off.

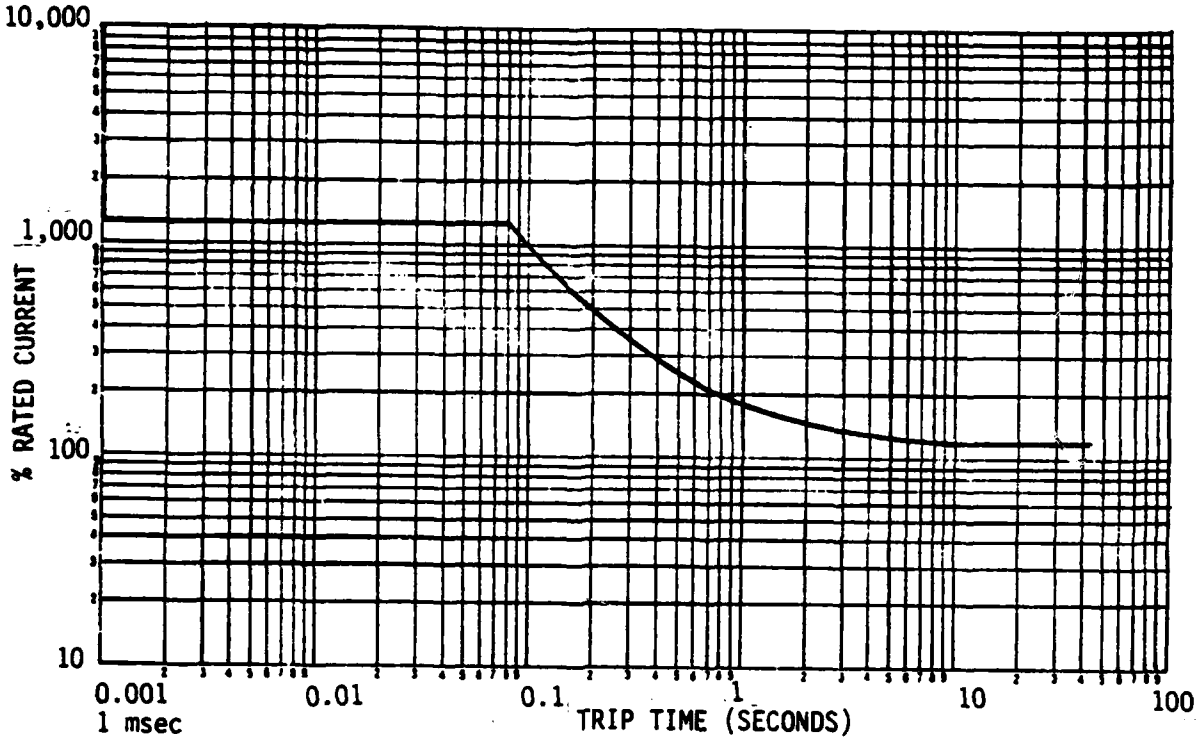


Figure 2. Rated Current vs. Trip Time

The Monolithic Solid-State Power Controller contains Analog and Digital circuits positioned on the monolithic device as shown in Figure 3, Monolithic apportionment.

These circuits are:

Analog	Digital
ADC Comparator	Up/Down Counter
Gain of 20 Amplifier	Shift Register
Comparator ZIC	Arithmetic Unit Accumulator
R-2R Ladder	Timer 5 mSec & 2.5 mSec
Switches	Mode Control
Comparator Voltage/Status	200 kHz Oscillator
	Clock Divider
	STAOT Status Logic
	5-Bit Counter

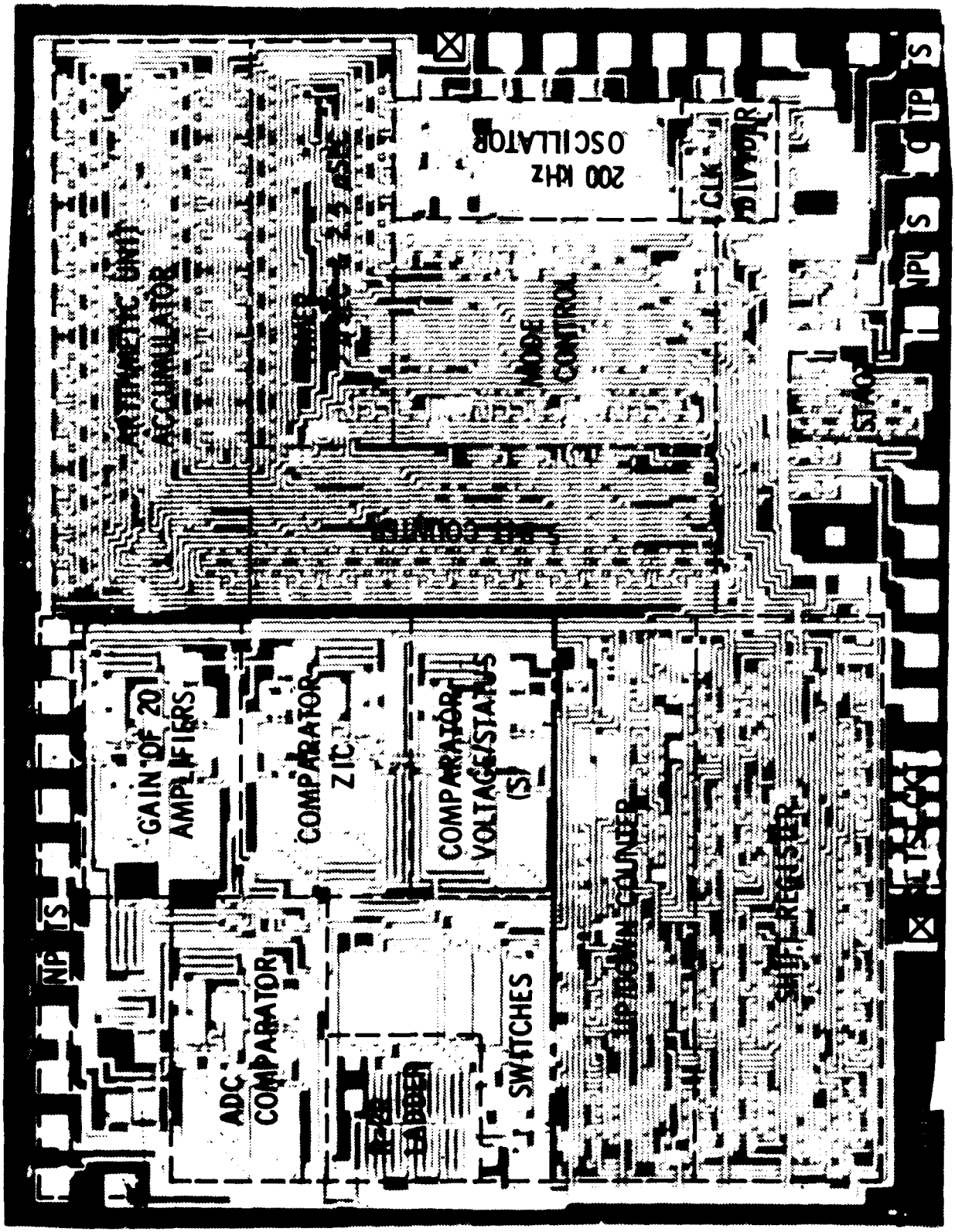


Figure 3. Monolithic Apportionment

Unique to the SSPC is the ability to combine large-scale integrated digital computing and analog signal processing on a single monolithic CMOS/SOS integrated circuit. The Analog Signal Processing includes conversion from analog to digital with a tracking type or counting converter as well as large (circa ±5 volts) and small (circa ±50 mv) signal threshold detection circuits with sufficient hysteresis incorporated to eliminate any crossover jitter problems.

A block diagram of the SSPC is shown in Figure 4 where the Mode Control is shown, for simplicity, as an exploded Veitch diagram.

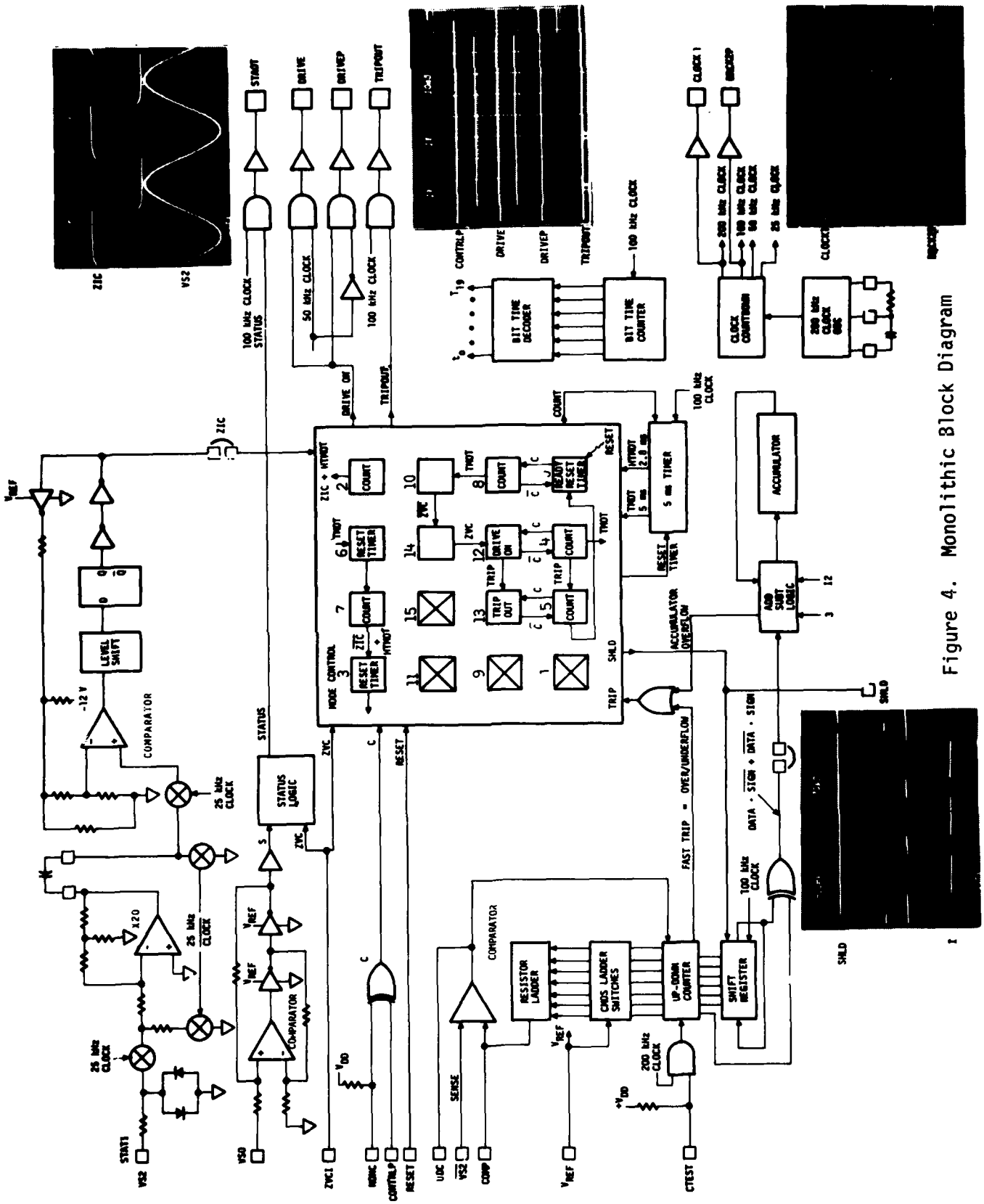


Figure 4. Monolithic Block Diagram

ANALOG-TO-DIGITAL CONVERTER

The on-chip Analog-to-Digital Converter consists of an analog comparator, an R-2R resistor ladder, seven analog ladder driver switches, a seven-stage up-down counter, a six-bit recycling shift register and logic to approximate the absolute value of the shift-register output.

Figure 5, the ADC Block Diagram, shows the interconnection of each of the components of the ADC. The ADC tracks the voltage applied to the SENSE INPUT and provides a serial output (I) that represents the absolute value of the SENSE INPUT.

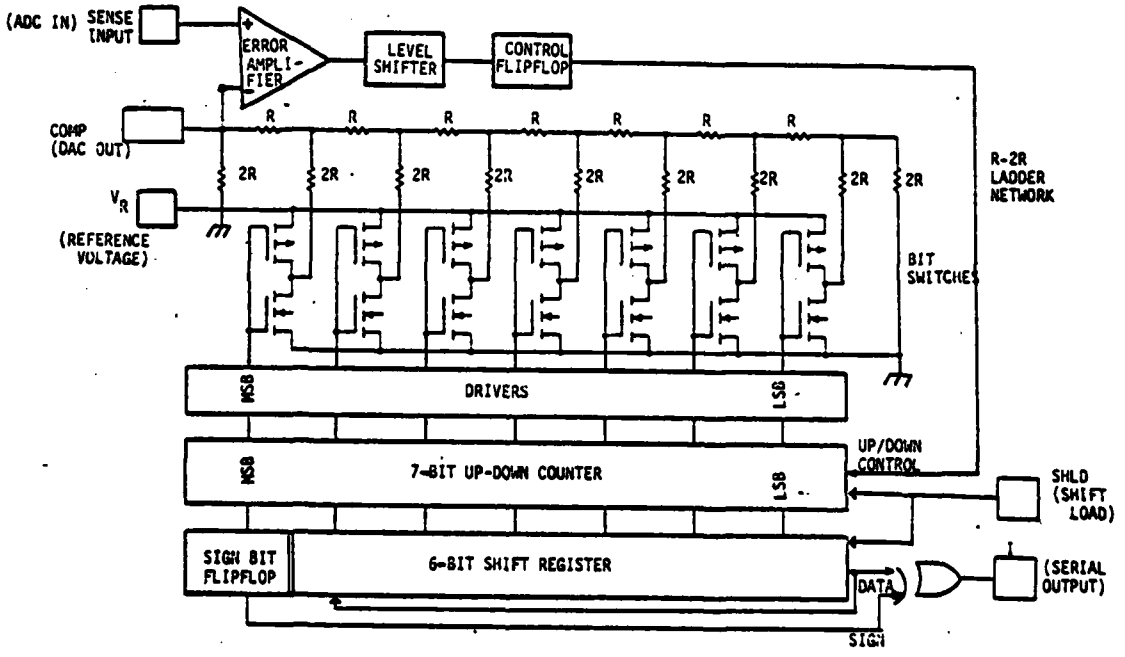


Figure 5. 7-BIT CMOS/SOS ADC

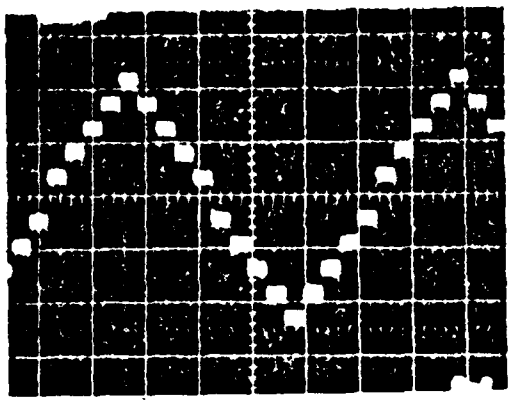
In the comparator, decisions are made as to the magnitude of the SENSE INPUT compared to COMP, the output of the R-2R ladder network. The comparator then commands the up-down counter to increase or decrease its binary count (and therefore the output of the ladder) until the two are within the resolution ($\pm$1 bit) tolerance. Waveforms depicting the tracking response of the ADC are shown in Figure 6.

Under control of the Shift-Load Control, SHLD, the magnitude of the up-down counter is transferred to the Parallel-to-Serial Register (6-bit shift register) while the sign bit is transferred to a separate flipflop. When the shift register is not loading, it is continuously shifting LSB first into an exclusive OR gate and back into its MSB end. The exclusive OR of the data and the sign provides a serial output, I, that approximates the absolute value of the ADC output. This is actually the one's complement of the measured instantaneous load current.

Scaling of the ADC is such that plus full scale is +6 volts and minus full scale is 0 volts. The resolution or value of the least significant bit is 3/64 volts. Any sense input, equal to or greater than, +6 volts or less than or equal to 0 volts will effect a fast trip. The ADC bit values and shift register I values for SENSE INPUT voltages are shown in Table I , Sense Input/ADC Scaling.

Two interface pins are available for functional test of the chip before it is packaged. These pins, CTEST and SHLD, may be useful to the potential designer because they provide control and monitoring capability over the ADC.

MAJOR CARRY

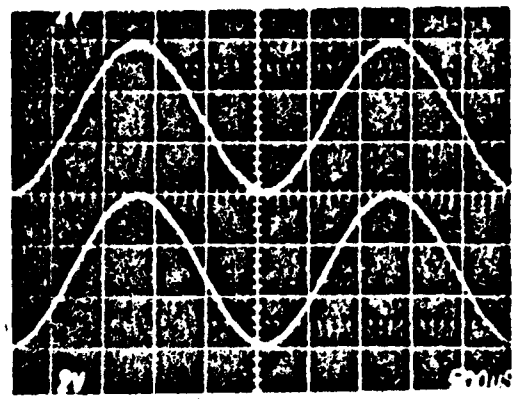


DAC OUTPUT (COMP)

2 ms/DIV

670 Hz CLOCK TRIANGLE INPUT

FULL SCALE 400 Hz



DAC OUTPUT (COMP)

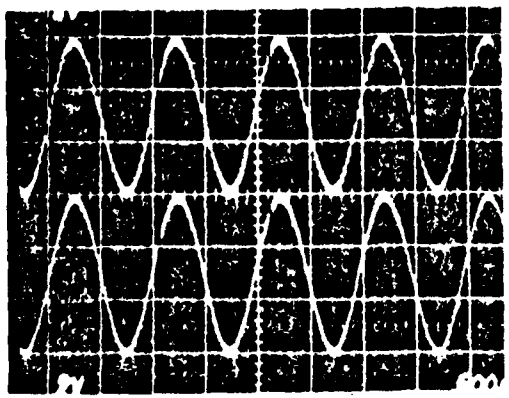
2 V/DIV

ADC (SENSE) (VS2) INPUT

500 µs/DIV

200 kHz CLOCK 400 Hz INPUT

1 MHz CLOCK 1 kHz SIGNAL



DAC OUTPUT (COMP)

2 V/DIV

ADC (SENSE) (VS2) INPUT

500 µs/DIV

Figure 6. ADC Tracking Response

Table I.

SENSE INPUT/ADC SCALING

SENSE INPUT VOLTS (INSTANTANEOUS)	ADC COUNT BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	SHIFT REGISTER I BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	COMMENTS
6.000	1	1	1	1	1	1	1	1	1	1	1	1	1	AUTOMATIC FAST TRIP
5.953	1	1	1	1	1	1	0	1	1	1	1	1	0	ADD
4.501	1	1	0	0	0	0	0	1	0	0	0	0	0	ADD
3.750	1	0	1	0	0	0	0	0	1	0	0	0	0	ADD
3.375	1	0	0	1	0	0	0	0	0	1	0	0	0	ADD
3.191	1	0	0	0	1	0	1	0	0	0	1	0	1	I2 ADD
3.188	1	0	0	0	1	0	0	0	0	0	1	0	0	SUBT
3.094	1	0	0	0	0	1	0	0	0	0	0	1	0	SUBT
3.047	1	0	0	0	0	0	1	0	0	0	0	0	1	SUBT
3.000	1	0	0	0	0	0	0	0	0	0	0	0	0	SUBT
2.953	0	1	1	1	1	1	1	0	0	0	0	0	0	SUBT
2.906	0	1	1	1	1	1	0	0	0	0	0	0	1	SUBT
2.959	0	1	1	1	1	0	1	0	0	0	0	1	0	SUBT
2.766	0	1	1	1	0	1	1	0	0	0	1	0	0	SUBT
2.719	0	1	1	1	0	1	0	0	0	0	1	0	1	I2 ADD
2.578	0	1	1	0	1	1	1	0	0	1	0	0	0	ADD
2.203	0	1	0	1	1	1	1	0	1	0	0	0	0	ADD
1.453	0	0	1	1	1	1	1	1	0	0	0	0	0	ADD
0.047	0	0	0	0	0	0	1	1	1	1	1	1	0	ADD
0.000	0	0	0	0	0	0	0	1	1	1	1	1	1	AUTOMATIC FAST TRIP

CTEST is a control gate that allows external control of the ADC clock. Such control allows the user to stop the ADC count or tracking while the shift register continues to be loaded and recirculated.

SHLD is the signal that causes the shift register to be loaded from the ADC up-down counter. The signal may be used for synchronization to permit observation or use of the Serial Output I. The waveforms in the lower left corner of Figure 4 show the I output relative to the SHLD test point. These are measurements from an actual device.

ERROR AMPLIFIER ADC COMPARATOR

The Error Amplifier is a high speed CMOS/SOS Analog Comparator. An unusual feature of the gate input on the CMOS/SOS analog comparator (see Figure 7) is that it can swing above and below the supply levels owing to the isolation of the input-gate oxide and the dielectric provided by the sapphire. Also, the protection circuit will afford ±17 volts before Zener action begins. Consequently, fault surges will not damage the comparator (SENSE) input.

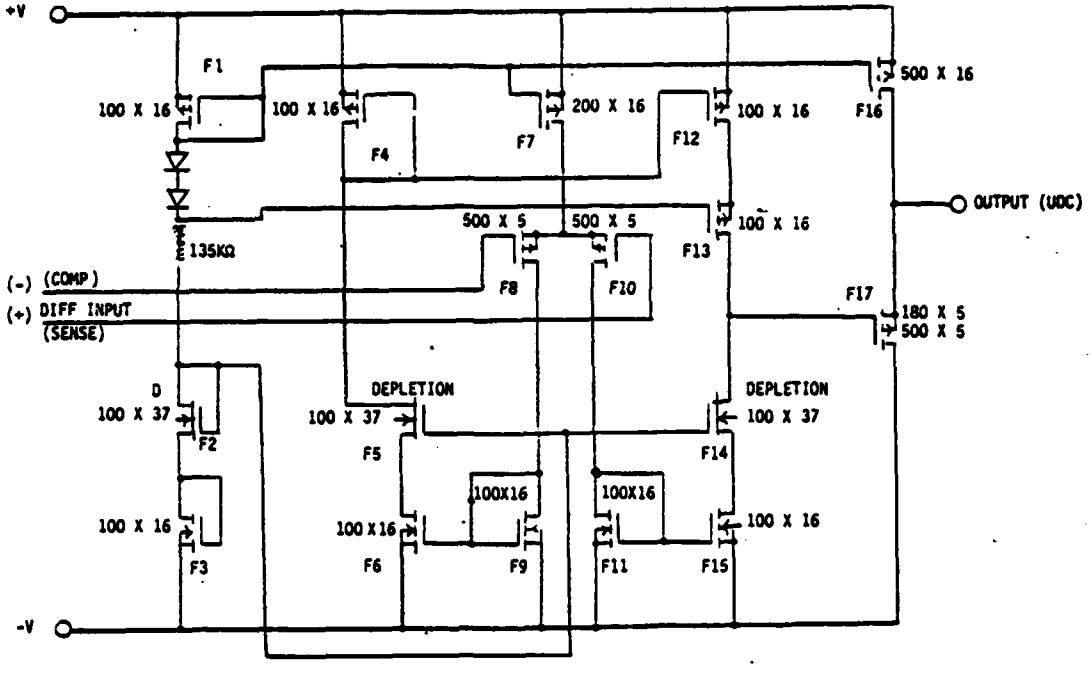


Figure 7. CMOS/SOS Analog Comparator

The Analog-to-Digital Converter (ADC) speed is limited by the settling time of the R-2R ladder network and the response of the comparator circuit. In CMOS/SOS, the sapphire affords minimum parasitic capacitance so other device circuit constraints will be required to enhance speed.

The comparator input-gate capacitance is small and reduces the load capacitance on the R-2R ladder output. However, the comparator-differential input stage uses a large-geometry F.E.T. to provide high gain. To offset the resulting capacitance loading on the output of the R-2R ladder network, the resistance value of "R" is reduced with the trade-off of increased power dissipation and greater area required for the switching F.E.T.'s. Two unique circuit features in the on-chip ADC make this speed power design trade-off optimum.

The first circuit feature is the use of depletion mode N-channel F.E.T.'s in the second-level gain stage of the comparator. This provides the large voltage gain required to obtain 80 db gain into the output source follower. The load line of the depletion F.E.T. is operated in saturation such that its drain-characteristic curve is flat. Further flattening of the operating characteristics of the depletion mode F.E.T. is obtained by placing an N-channel F.E.T. (F15 in Figure 7), designed for high gain, in series with the 12 volts. This gate is coupled to the first-stage differential conversion load F11. Both sides of the differential amplifier are coupled to high-gain N-channel F.E.T.'s in series with the depletion mode N-channel F.E.T. As a result, the complement of the input is available for the coupling to the P-channel gate F12 which provides the push-pull drive needed to make the comparator output swing both positive and negative. It should be pointed out that the high-gain stage being after the differential input affords minimum gate-input capacitance of 1 pfd. To reduce the required output voltage change, a level shifter (see Figure 5) which requires a +3 volt input to provide +12 volt Logic "1" output is used. Logic "1" results when the comparator output is less than +3 volts. A control-flipflop Up-Down Control (UDC) is used

to synchronize the up-down control for the counter based on the required polarity difference between the R-2R ladder output and the sense input to the comparator. Thus, the ADC is the tracking type which continuously counts either up or down based on the high-gain comparator output and the period of Clock #1 (200 kHz).

The second circuit feature of the ADC is the delay stage in the bit switches which delays the large P-channel switch turn-on until the N-channel switch is turned "OFF". Significant power savings result by eliminating the dc path created in normal large inverter switches when both F.E.T.'s are simultaneously in their linear region of operation. Also, by eliminating this current spike, a higher impedance filter may be used with ADC reference supply.

The high-gain differential amplifier circuit that is used for the ADC Error Amplifier, Figure 7, is also used in the following functions: Voltage Status Input Amplifier (see STATUS), the Level Sensor for Low Level Current or Voltage Sensor and in the Chopper Stabilized Gain of Twenty Amplifier (see ZIC). It should be pointed out that the feedback network which establishes the gain of twenty imposed additional internal frequency compensation requirements. A high-frequency roll-off was achieved using a capacitor to ground on the input to the source follower (F17).

ZIC

The VS2 (STATI) input, a voltage that is proportional to instantaneous load current, is amplified with a chopper stabilized X20 amplifier and the result is compared to a reference. The reference changes in value with the results of the comparison. The upper right hand corner of Figure 4 shows the measured waveforms from an actual device and the relationship of the ZIC output to the VS2 input. Figure 8 is a more detailed schematic of the ZIC circuitry. Once the output (ZIC) is zero volts (logic zero), the input (VS2) must go more negative than -16 mv before the output will switch to positive 12 volts (logic one). When the output is at +12 volts (logic one), the input must go more positive than +15 mv before the output will switch back to zero volts (logic one). The ZIC term is used in the control logic as a condition for turn-off of the pass elements for ac power control.

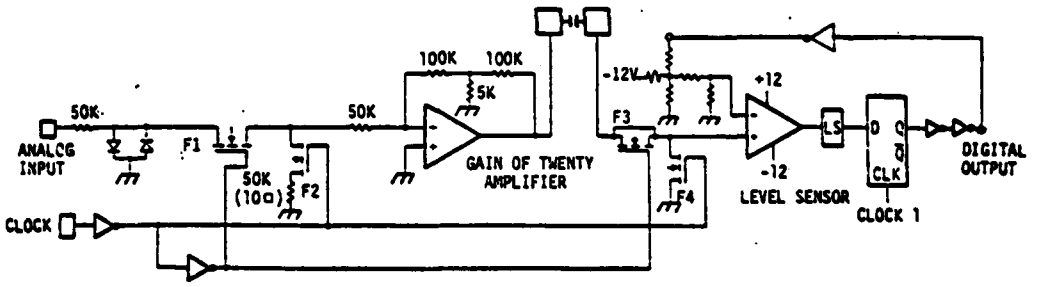


Figure 8. Monolithic Device - Linear Section - ZIC Loop

Chopper stabilization removes drift problems at high temperature and provides dc restoration for the threshold differential amplifier (Level Sense). The chopping function is accomplished with small geometry N-channel F.E.T.'s (F1, F2, F3, and F4) as shown in Figure 8. A 25%-duty-cycle clock is used to afford the major portion of the 25 kHz clock cycle for dc restoration. Although the coupling capacitor is external in this design, it could now be included on the CMOS/SOS integrated circuit.

STATUS

The Status mechanication utilizes both linear and digital techniques that are imbedded in a singular monolithic CMOS/SOS integrated circuit. The VSO input is used as representative of the load voltage and is compared with ZVC, which is representative of the line voltage, to indicate that full-wave voltage is applied to the load. The VSO input is applied to the input of a comparator circuit that employs hysteresis, as shown in Figure 9. A resistive voltage divider produces 5 volts peak at VSO when the ac line voltage is near 70% of the rated line voltage. When the output, S, is high (+12 volts), VSO must go to -5 volts before the output will switch to high. The Sterm, via the hysteresis described above, provides a square wave at the frequency of the line voltage. A phase relationship between S and ZVC is provided because ZVC switches at zero line voltage and S switches near 70% of the peak load voltage.

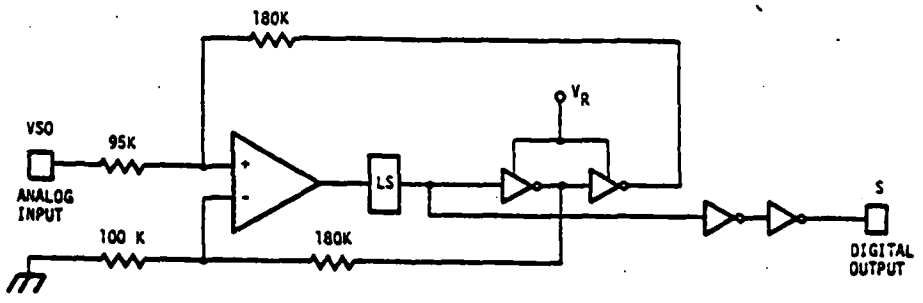


Figure 9. Monolithic Device - Linear Section - Voltage Status

The phase relationship between ZVC and S is used to verify that both half cycles of the ac are present and are at the proper amplitude. The status logic compares the S term with ZVC. If S is always true (high) when ZVC goes from high to low and S is always false (low) when ZVC goes from low to high, then full wave power is applied to the load and the Status Output (STAOT) will be true. If S stays in one state or the other due to improper load voltage, amplitude, or half-cycling of the load voltage, then STAOT will be false. Figure 10 shows the logical arrangement and timing diagram of the circuitry used to provide STAOT. Note that STAOT will be way related to the command or mode control; therefore, shorted or failed switching of the ac output is indicated as STAOT true when the controls are off, a form of built-in diagnostic testing.

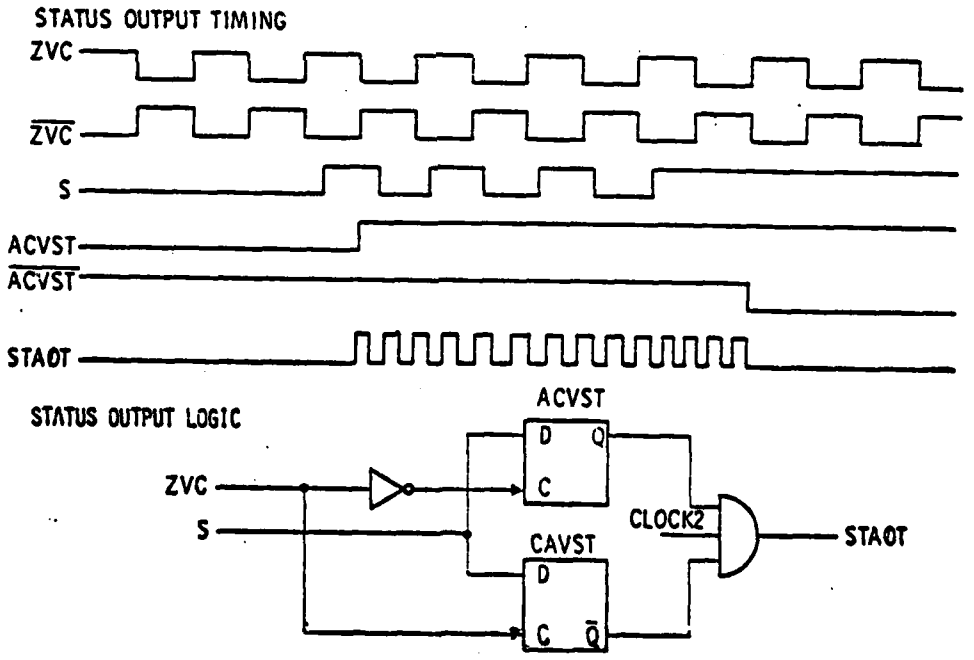


Figure 10. STAOT Logic & Timing

MODE CONTROL

Measured waveforms of the timing relationship of control prime (CONTRLP), drive, drive prime (DRIVEP), and tripout are shown in the right center edge of Figure 4. These waveforms, triggered on the leading edge of CONTRLP, show the 5-to-7.5 msec delay between the on-command and the beginning of the 50 kHz chopped DRIVE and DRIVEP outputs.

The 5-to-7.5 msec delay is made up as follows:

1. 5 msec TIME DELAY of the Mode Control is used to insure that the CONTRLP change is valid and not just a transient.
2. 0-to-2.5-msec wait for the correct zero-voltage crossing (ZVC).

Additionally, the timing relationship between the drive signals and the trip indication (TRIPOUT) is shown.

Figure 11 is a sequence flow diagram that will illustrate the sequence of operations that occur and are controlled by the MODE CONTROL. The MODE CONTROL, or sequencing, is shown in logic diagram form in Figure 12. The major functions to be described are Turn-On, Turn-Off, Trip, and Reset After Trip. The sequence of operations will be described in terms of the logic state diagram and movement from box # to box #. The box #'s may be followed in the VEITCH Diagram in the mode control portion of Figure 4.

When primary power is applied to the monolithic circuit, all mode controls and counters are required to reset to a READY or standby mode (top of Figure 11). This is the lower right of Logic State Diagram in Figure 4, or Box 0.

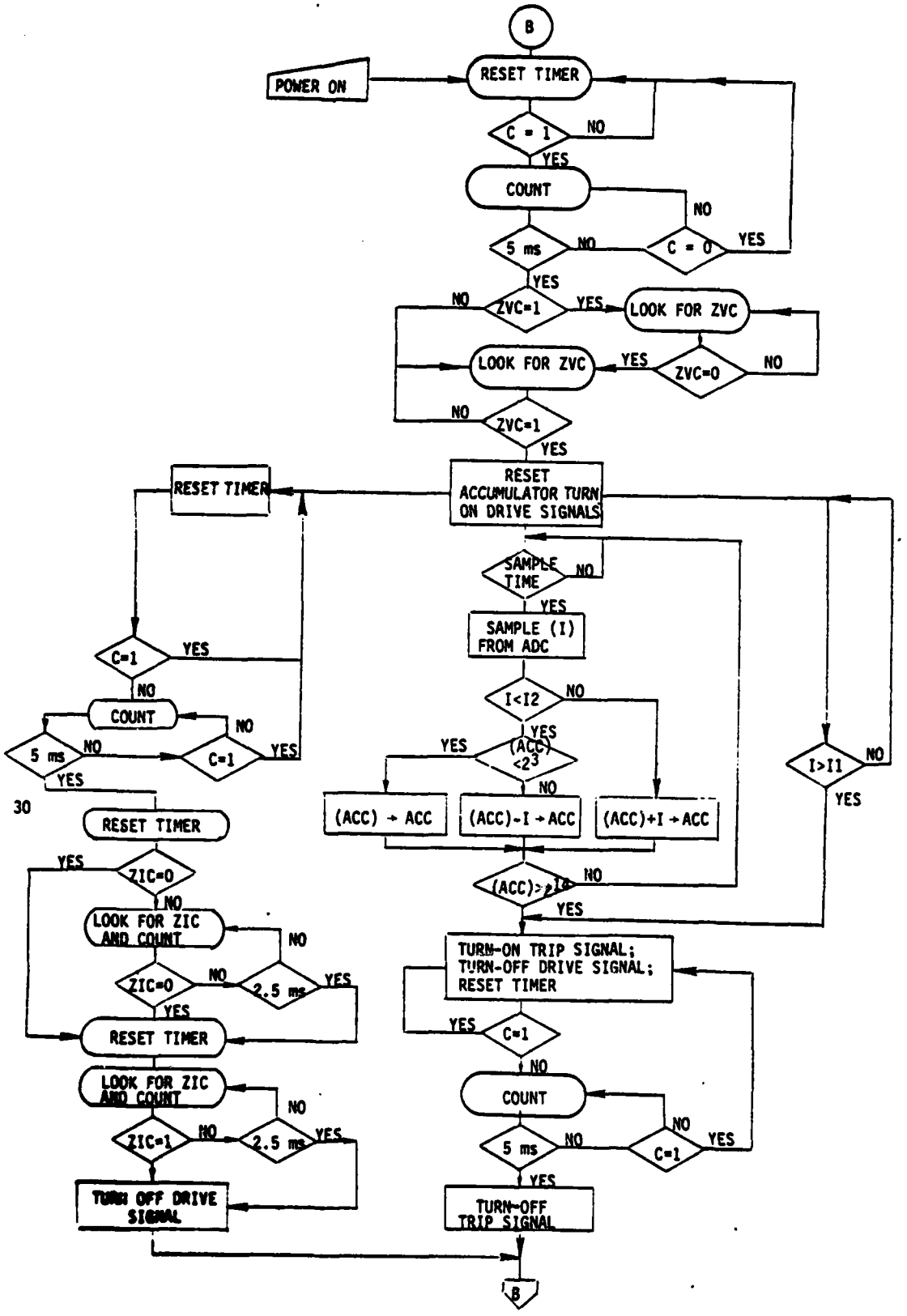


Figure 11. Sequence Flow Diagram

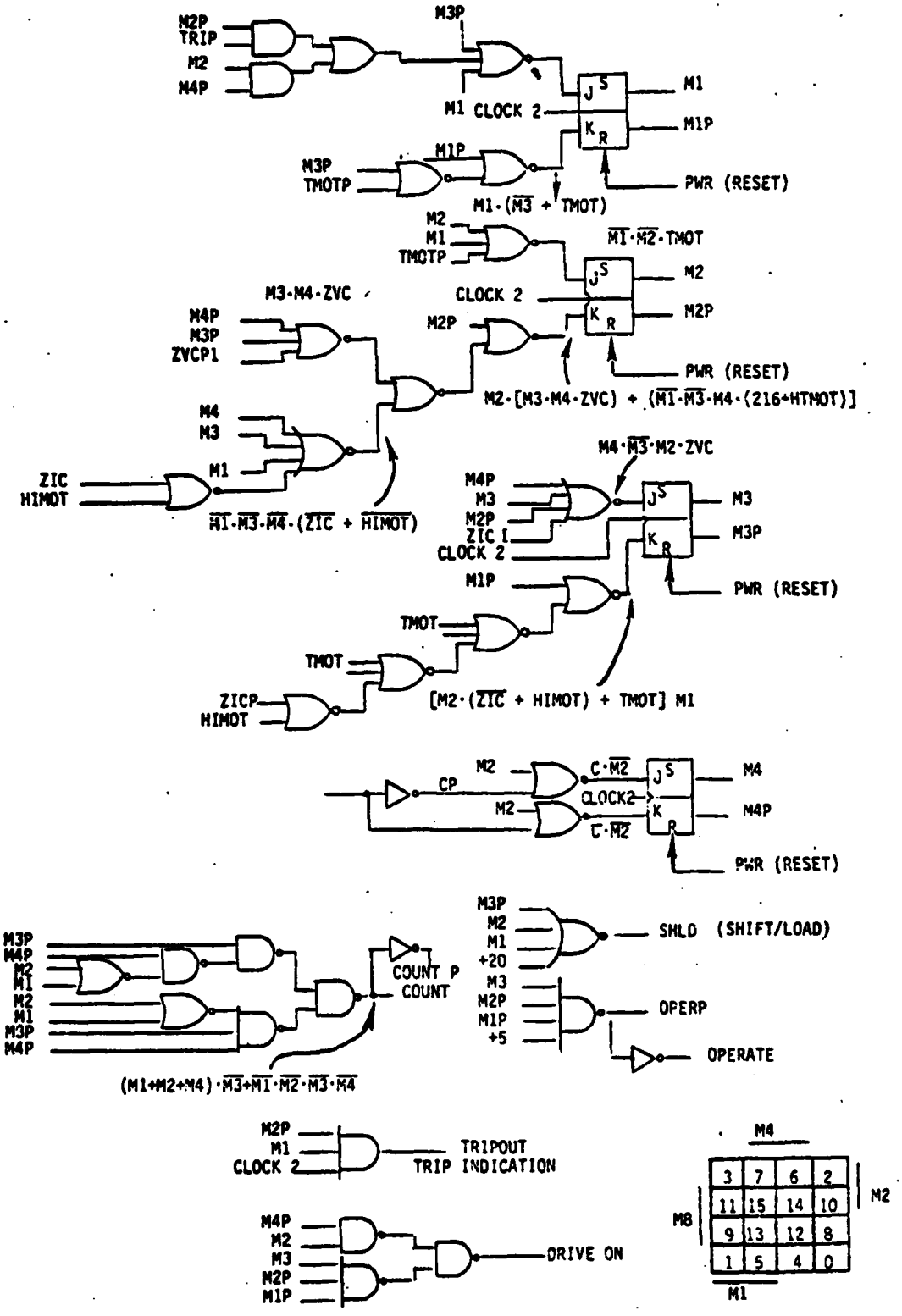


Figure 12. Mode Control Logic Diagram

The input logic terms that command the on-off condition of the SSPC are CONTROL, NONC, and ZVC. CONTROL is a logic signal that initiates the turn-on/turn-off sequence and the NONC term specifies the specific logic state (high or low) that will initiate turn-on (e.g. for NONC high, a control low will initiate turn off; likewise, for NONC = low, a control high will initiate turn on and control low will initiate turn-off.)

The third term, ZVC, is the final condition for turn on and is not involved in turn-off. Turn-off uses ZIC, developed internally and not a logic input, as a final condition under normal circumstances. Under trip, or overcurrent conditions, the ZIC is ignored in the turn-off sequence.

TURN-ON

The discussion of the operation will center around the term C rather than control. The term C is used to control the turn-on/turn-off and reset-action after trip. It is to be developed as an EXCLUSIVE OR of the CONTROLP term and the NO/NC term. This logical operation is permitted so that the SSPC can be commanded to be normally off (open) or normally on (closed) by an external jumper.

A pull-up resistor is included so that the circuit with no jumpers will operate in the normally open (NO) mode. When the NO/NC term is externally jumpered to VS1, the circuit will operate in the normally closed (NC) mode. The following truth table describes the desired operation.

C TRUTH TABLE

CONTROLP	NO/NC	C
0	0	0
1	0	1
0	1	1
1	1	0

C = 1, turn-on drive lines in the prescribed sequence
C = 0, turn-off drive lines in the prescribed sequence
NO/NC = 0, VS1 ground jumpered to NONC
NO/NC = 1, NONC left open-circuit (no jumper)

If C is detected as a logic true, the Mode Control (MC) will move from Box 0 to Box 8 and a five-millisecond timer is started and continuously compared with C, to assure that C remains true for a full five milli-

seconds. If C does not remain true, MC will move back from Box 8 to Box 0. After the five milliseconds have elapsed, with the C term remaining true, MC moves from Box 8 to Box 10 and waits for ZVC to be low. When ZVC is low, MC moves from Box 10 to Box 14, waiting for the beginning of a positive half cycle of the line voltage. The next positive edge of the ac line voltage forces ZVC true and causes MC to move from Box 14 to Box 12 which causes the DRIVE outputs to be enabled, turning the SSPC "ON". With the DRIVE outputs on, three alternate operating modes are possible. These are overcurrent fast-trip,(X in Figure 11), timed overcurrent-trip, (Y in Figure 11), and normal turn-off by removal of the C term (Z in Figure 11).

TURN OFF

For special application reasons involving square-loop magnetic loads and electromagnetic interference, it is required that ac line voltage be disconnected from the load when the load current is zero with a positive slope. (This completes an integral number of cycles.) The normal mode of turn-off is accomplished by removal of the C term. When C is removed, MC moves from Box 12 to Box 4, and the five-millisecond timing sequence is started. Upon completion of the 5-msec-time out (TMOT), MC moves from Box 4 to Box 6. The control logic begins to look for a negative half cycle of the load current. The Zero-Current Crossing (ZIC) signal is true during the negative half cycle and false during the positive half cycle of the load current. When the five-millisecond timing sequence is completed and MC goes from Box 4 to Box 6 to Box 7, the control logic will look for a positive half cycle ($\overline{ZIC}$) and simultaneously start a 2½-millisecond timing sequence. When ZIC is false or when the 2½ msec timer completes its time (HTMOT), the MC will move from Box 7 to Box 3, where the timer is again reset and MC moves immediately to Box 2. In Box 2, the control logic will look for ZIC to be true and simultaneously restart the 2½-msec timing sequence. When ZIC is true or when HTMOT is true, the MC will move from Box 2 to Box 0. At this point, the ac line has just started a negative half cycle. This will remove drive to the Series Pass Element and extinguish the load current.

TMOT = Time Out 5 msec
HTMOT = Half Time Out 2½ msec

Drive outputs are on when MC is in Boxes 4, 12, 6, 7, 3 or 2.

TRIP

Overcurrent Fast-Trip - Once the DRIVE outputs are on, Box 12 or Box 4, the instantaneous sensed values of the current (I) being delivered to the electrical load are digitized by the ADC and compared to a constant I1, where I1 represents a catastrophic overcurrent situation, and in this case, is full scale (plus or minus) of the ADC. If I1 is exceeded in magnitude, the DRIVE outputs are immediately disabled and a trip output is generated (Fast Trip). MC moves from Box 12 to Box 13 or from Box 4 to Box 5.

Timed Overcurrent-Trip - If, while in Box 12 or Box 4, any value of I (the absolute value of the digitized, instantaneous load current) equals or exceeds I2 (a digital constant that represents the minimum current value that will be accepted and added to the accumulator), the accumulator will increase in value. The accumulator will add values of I that are equal to or greater than I2 and will substract values of I that are less than I2. The value of I2 is set at 2^2 plus 2^0 (5 counts) as shown in Table I. When the input is sinusoidal and has an rms value greater than or equal to $\frac{15}{64\sqrt{2}\sin 60^0}$ volts, with a dc offset of +3 volts, the accumulator sum (or contents) will be larger at the end of a cycle than it was at the beginning of a cycle. When the input signal is less than $\frac{15}{64\sqrt{2}\sin 60^0}$ volts rms with a dc offset of +3 volts, the accumulated sum (or accumulator contents) will be less at the end of a cycle than it was at the beginning of the cycle.

When the accumulator contents are $\geq 2^{14}$, the current vs. time relationship shown in Figure 2 has been satisfied and a timed trip output is generated. This will cause the Mode Control to move from Box 12 to Box 13 or from Box 4 to Box 5. DRIVE outputs will be disabled and a trip output will be generated.

RESET AFTER TRIP

After entering the tripped state via Fast Trip, or by Timed Trip, the monolithic circuit must remain in this tripped state and the TRIP output must remain true until the term C has been removed. A Trip output is generated when MC is in Box 5 or Box 13. If C is removed, MC moves from Box 13 to Box 5 and a five-millisecond counter timer is started. If C goes true again, MC will return from Box 5 to Box 13 and reset the timer.

When MC is in Box 5 and the timer completes its 5-msec time out (TMOT), the MC moves from Box 5 to Box 0, where the TRIP output is reset, and all mode controls and counters are reset, returning the circuit to the READY mode.

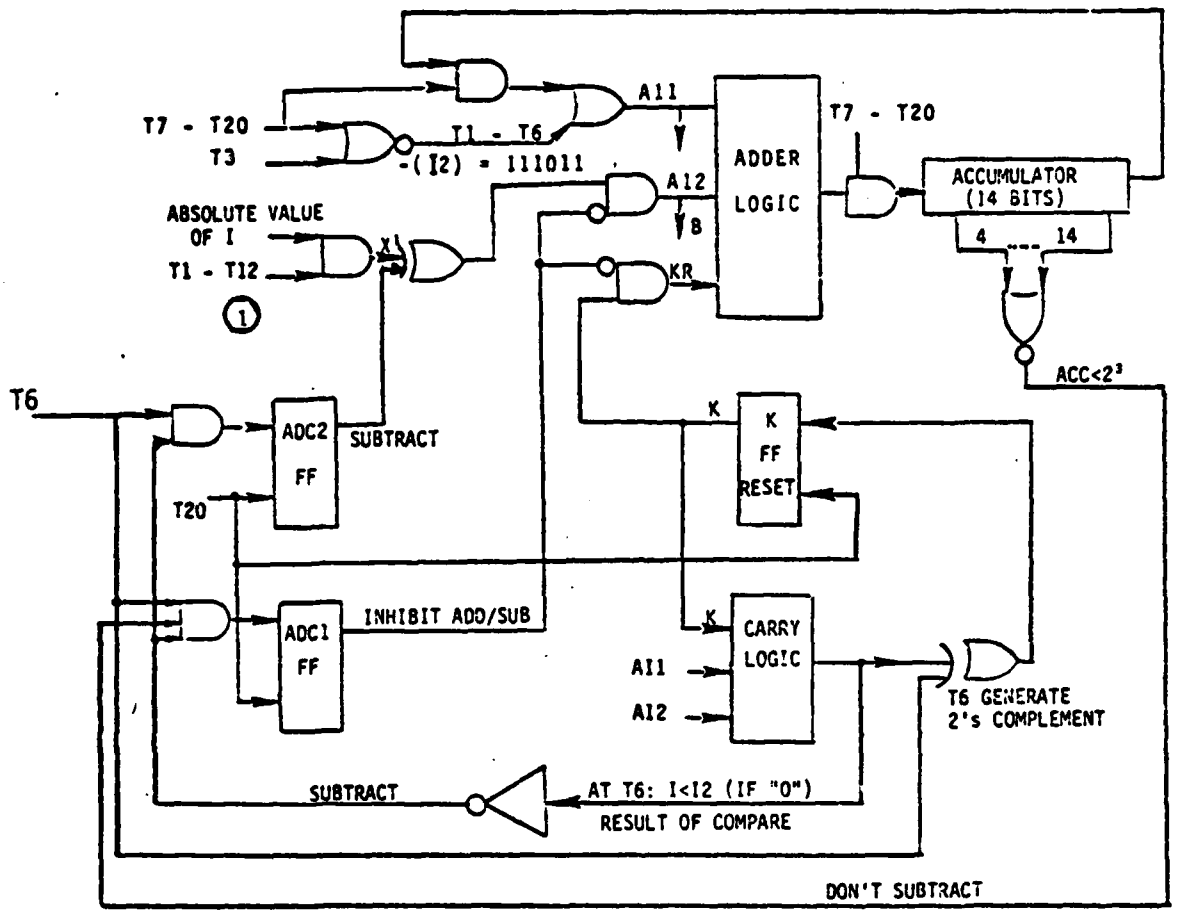
The above paragraphs outline the primary functions of the Solid-State Power Controller, which are Turn-On, Turn-Off, Trip and Reset After Trip. Additionally, interfaces are provided to indicate the on or off condition of the SSPC (STATUS INDICATION) and the condition of the Trip Off Logic (TRIP INDICATION).

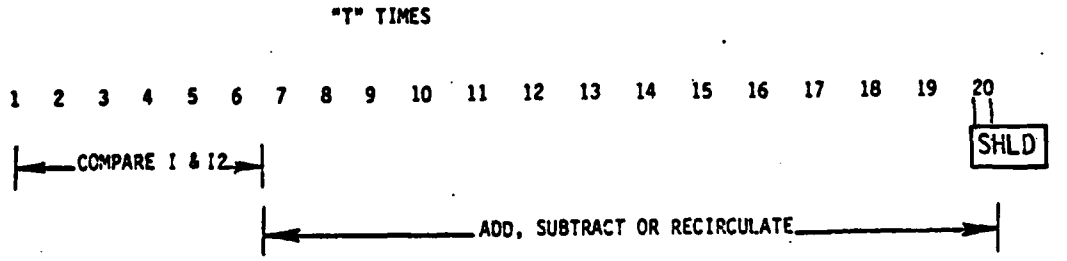
DIGITAL FILTER AND TRIP TIME COMPUTATIONS

It is convenient to think of the digital filter structure as a hardware configuration made up of a Shift Register and an Arithmetic and Control Unit. This is shown in the Logic Diagram of Figure 13. Figures 12 and 13 are included for the expert logicians and are not necessary to understand the operation of this device. Mechanization of a digital filter requires that past values of the output, input, and intermediate sequences be available. This implies a means of delay or switch which, in the SSPC device, has been accomplished by the two Shift Registers operating in a recirculating mode. These Shift Registers are inhibited from recirculating when the ADC Up-Down Counter is parallel loaded into the Shift Register every 200 μsec. This is during SHLD.

In simplified block diagram style and more in the form normally used with digital filters, Figure 14 shows the shift registers and arithmetic logic that are used to mechanize the digital-filter style, trip-time computations. The I Shift Register is described in the ADC section of this report and is loaded from the ADC Up-Down Counter at the last bit time of the machine cycle (SHLD time).

The I Registers (6 bits in length) is loaded from the ADC at T_{20} (SHLD) and continuously recirculates for the entire 20 bit cycle. The results (of the 20-bit shift in a 6-bit shift register) are not to be used during the last 8-bit times and, therefore, the odd shift pulses do not upset the computations.





AT T6
- SET ADC2 FOR ADD/SUBTRACT
- SET K FOR ADD/SUBTRACT INITIALIZE
- SET ADC1 FOR RECIRCULATE IF ADC<2³ & I<I2

(1) T13 - 20, X^1 = 0 IF ADC2 = 0 ∴ ADD
X^1 = 1 IF ADC2 = 1 ∴ SUBTRACT

Figure 13. Arithmetic Unit Logic Diagram

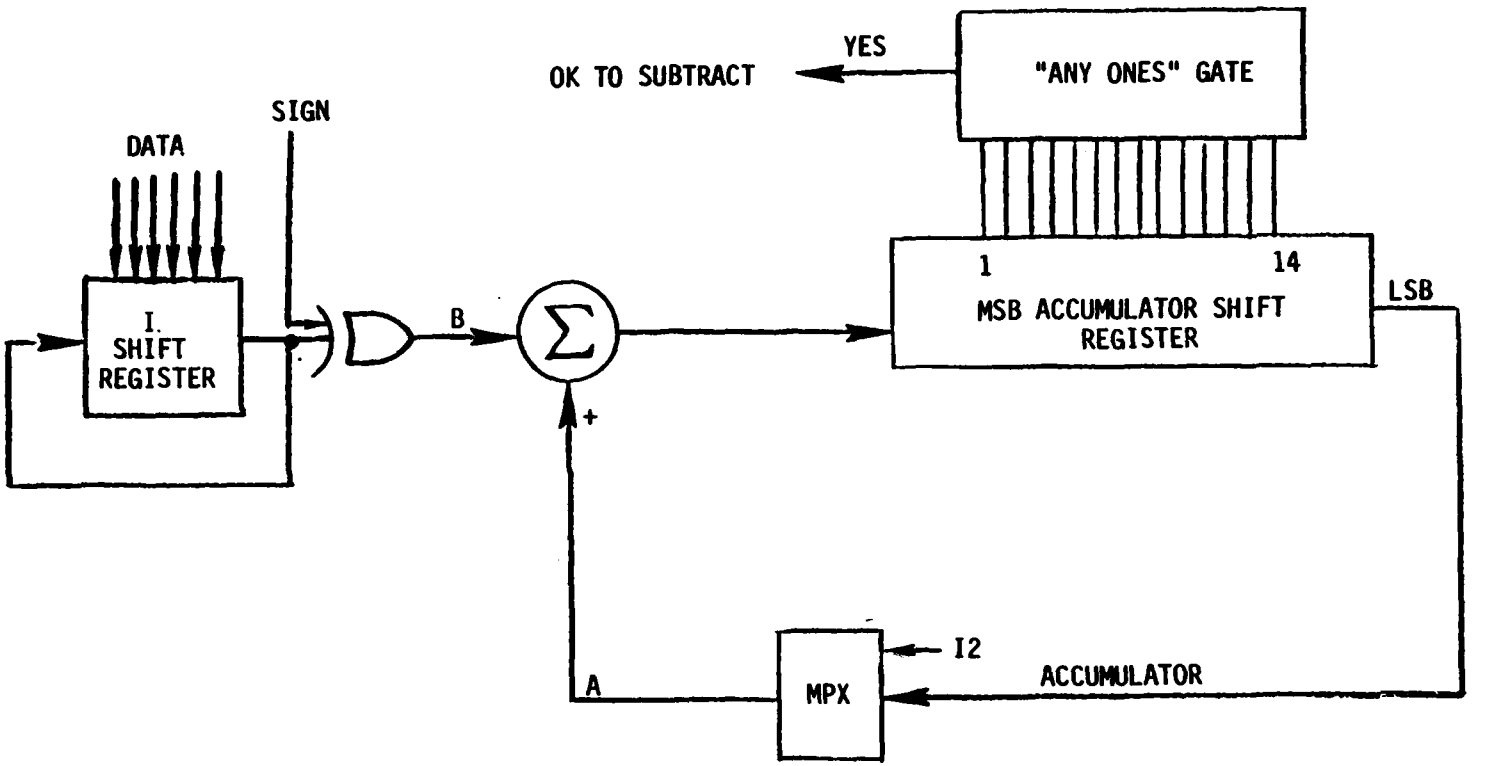


Figure 14. Shift Registers & Arithmetic Logic Block Diagram

A = I_2 During T_1 Thru T_6

A = Accumulator During T_7 Thru T_{20}

B = I During T_1 Thru T_6

B = -I During T_7 Thru T_{12} & 1 During T_{13} Thru T_{20} IF $I < I_2$ & OK To Subtract

B = 0 During T_7 Thru T_{20} IF $I < I_2$ & Not OK To Subtract

B = I During T_7 Thru T_{12} & 0 During T_{13} Thru T_{20} IF $I \geq I_2$

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The first 6-bit times after the load (T_1 - T_6) are used to subtract I_2 from I. If, at T_6, the carry logic is zero, then $I < I_2$ and subtraction, for the next 14-bit times, may be in order. The value of the accumulator is then checked for "1's" in the 11 most significant bits. If the accumulator contains a value larger than 2^3 (any "1's" in the upper bits positions), the I value is subtracted from the accumulator and the result put in the accumulator (this occurs during bit times 7 through 20). The subtraction process allows the accumulator to decay to near zero level if an overload occurs and then disappears. If there are no "ones" in the upper accumulator, the accumulator recirculates with no change.

If, at the end of T_6, the carry logic is true, then $I \geq I_2$ and addition, for the next 14-bit times, is in order and I plus the accumulator contents is stored in the accumulator during bit times T_7 through T_{20}.

If at the end of T_{20} the carry logic is true, then the accumulator has overflowed, i.e. accumulator contents $\geq 2^{14}$ and the Timed Overcurrent-Trip sequence is completed.

200 kHz OSCILLATOR

The phase relationship of CLOCK1 (200 kHz) and DRCK2) (100 kHz) is shown in the lower right corner of Figure 4. Again, these are measurements from an actual working device.

A unique three-pin oscillator was developed for the SSPC to reduce on-chip power dissipation and to make the period of oscillation independent of process variations. A single external resistor and capacitor are used to determine the R-C time constant as shown in Figure 15. A second resistor normally used to limit the voltage swings at the timing node CT2 is not required because of Zener input protection being used rather than diodes. Thus, when the timing node swings higher than V_{dd}, the protection network will not clip the timing waveform and the frequency of oscillation is dependent upon the value of the external R-C components.

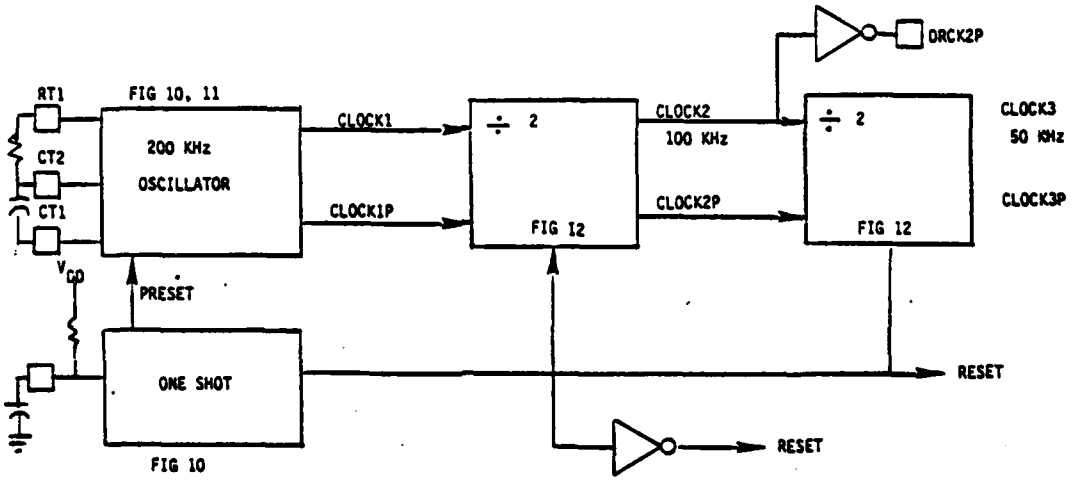

Figure 15. Oscillator Block Diagram